IEEE wai 2026

2026 International Workshop on Advanced Interconnects

Hangzhou, China

WAI 2026

November 4 – 6, 2026

Advance program



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Please contact our staff for more information：

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INVITATION FROM THE GENERAL CHAIRS

Dear Colleagues and Friends

On behalf of the 2026 WAI Steering Committee, we are privileged and honored to invite you, your colleagues and families to join us for the third International Workshop on Advanced Interconnects (WAI) from Wednesday, Nov. 4th to Friday, Nov. 6th in Hangzhou, China.

The International Workshop on Advanced Interconnects technically co-sponsored by the IEEE and the IEEE EMC Society is a newly launched event. The scope of this workshop specially addresses the latest development and innovations in the advanced interconnects field. The topics include but are not limited to: advanced interconnects and packaging, signal and power integrity, electromagnetic interference and compatibility (EMI/EMC), electrostatic discharge (ESD) and reliability, multiphysics integrity, modeling, simulation, and design methodologies, AI and intelligent EDA technologies, measurement, testing, and validation, as well as RF, microwave, antennas, and emerging applications and systems.

The IEEE EMC Society is the primary co-sponsor of this event, in collaboration with DetoolTech Ltd, Zhejiang University, Nanjing University of Aeronautics and Astronautics and China University of Petroleum.

We warmly welcome you to join us in Hangzhou in November of 2026 for an outstanding scientific/technical event and an unforgettable experience for you and your family.

WAI 2026 General Chairs



Er-Ping Li, IEEE Fellow

Qiushi Chair Professor, Zhejiang University



Jun Fan, IEEE Fellow

Qiushi Professor, Zhejiang University

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China



GENERAL INFORMATION

REGISTRATION

Registration link: https://wai-emc.com/wai2026/registration

Please register an account if new to the Registration site.

Each participant must pay a non-refundable registration fee. **Only registered and paid submissions before 26 October, 2026 will be scheduled in the symposium program.** Inclusion of a submission whether it is an abstract or a full paper in the final Technical Program is guaranteed only after the registration of one of the authors is completed and paid before 26 October, 2026, through the Registration link. **One paid registration can cover a maximum of two submissions.** The abstracts and full papers listed in the final Technical Program will be archived in the WAI 2026 Proceedings after they are presented in the conference, any absent submission will be removed. Further, the full papers archived in the WAI 2026 Proceedings will be further uploaded and archived in the IEEE Xplore (EI indexed).

On-site registration will be available through the Registration Desk during the workshop.

The same fee structure is used for both online and onsite registrations. Registration includes daily tea break, lunches and dinners from November 4 to November 5.

Registration Type	Registration Fee
Student Registration	USD 208 / RMB 1480
Regular Registration	USD 348 / RMB 2480

CONFERENCE VENUE

Hangzhou Blossom Water Museum Hotel (杭州宝盛水博园大酒店)

Hangzhou Blossom Water Museum Hotel is located on the banks of the world-renowned Qiantang River, within the China Water Museum Park in Hangzhou. The hotel is approximately 30 minutes from West Lake and only a short drive from Hangzhou Xiaoshan International Airport.

Surrounded by lush greenery, tranquil lakes, and the magnificent Qiantang River, the hotel provides a unique combination of river views, lake views, and garden landscapes. Covering an area of approximately 112 acres, the hotel has been carefully designed as a distinctive resort-style destination integrating natural scenery, comfortable accommodation, and conference facilities.

Its peaceful environment and convenient transportation make it an ideal venue for WAI 2026 participants.

杭州宝盛水博园大酒店坐落于举世闻名的钱塘江畔，中国水立博物馆园内。酒店距离西湖约 30 分钟车程，距杭州萧山国际机场也仅一小段车程。

酒店四周绿树环绕，静谧的湖泊与壮丽的钱塘江相映成趣，将江景、湖景与园林风光完美融合。酒店占地约 112 英亩，经过精心设计，打造成了一个集自然风光、舒适住宿和会议设施于一体的特色度假胜地。

这里环境宁静，交通也十分便利，是 WAI 2026 参会者的理想下榻之所。







LOCATION MAP AROUND THE CONFERENCE VENUE



★Hangzhou Blossom Water Museum Hotel

Address: No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China

(+86-571-83500888)

Website: https://www.hangzhoublossomwater.cn/

REGISTRATION DESK

Admission to all sessions and hosted functions requires the attendance identification. Please wear your name badge at all times.

Badge and other workshop materials can be picked up from the Registration Desk during the workshop for the participants registered online. On-site registration will also be available through the Registration Desk.

Registration Desk time

☐ November 3, Tuesday	14:00 - 19:00
☐ November 4, Wednesday	7:30 – 17:00
☐ November 5, Thursday	7:30 – 17:00
☐ November 6, Friday	7:30 – 9:00

Registration Desk will be located in the front lobby of the conference venue.

Hangzhou Blossom Water Museum Hotel

杭州宝盛水博园大酒店

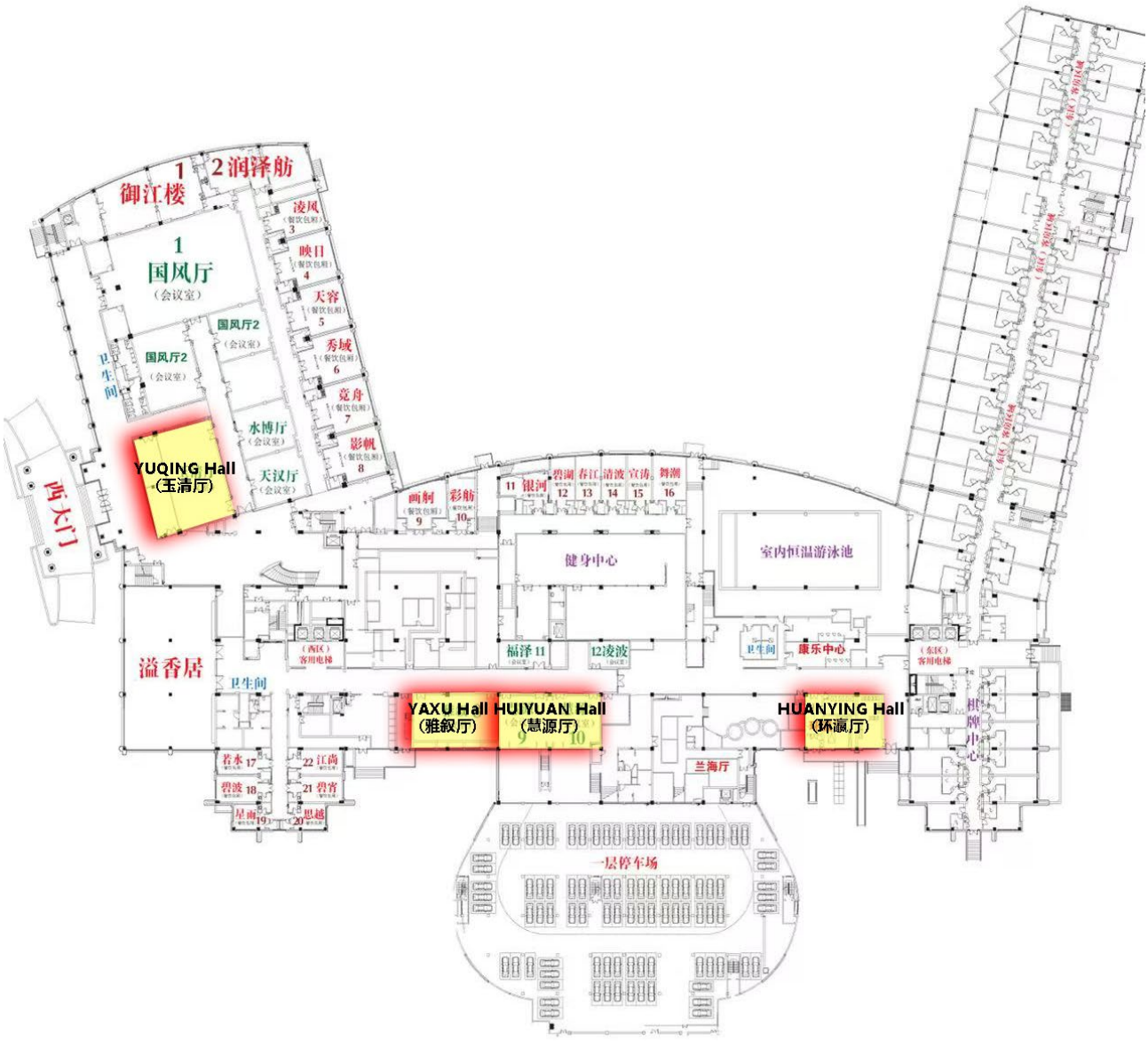
No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China



EXHIBITION HALL AND MEETING ROOMS

Opening Ceremony (开幕式及大会讲座)	BAOSHENG Hall @Level 2 (2 楼宝盛厅)
Parallel Sessions (分会场)	Room 1: HUANYING Hall @Level 1 (1 楼环瀛厅) Room 2: HUIYUAN Hall @Level 1 (1 楼慧源厅) Room 3: YAXU Hall @Level 1 (1 楼雅叙厅) Room 4: YUQING Hall @Level 1 (1 楼玉清厅) Room 5: QIER Hall @Zheda Yuanzheng International Hotel in Haining **(Round-trip shuttle service from Hangzhou provided)** (海宁浙大圆正国际酒店启尔厅，**提供杭州往返大巴接送**)

宝盛水博园大酒店(1F)平面图



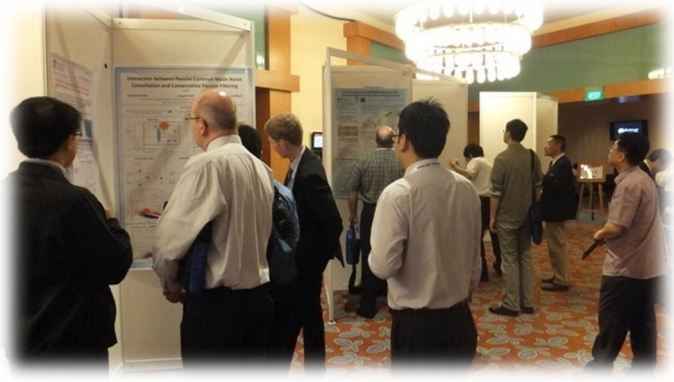
INSTRUCTIONS TO POSTER PRESENTERS

Poster Presentation

Poster sessions will be held at **YAXU Hall (雅叙厅).**
Please register at the Registration Desk before proceeding to locate your assigned poster board. To locate your assigned poster board, look for the board marked with your Paper ID.

Prepare your poster

- ☐ Each presenter is provided with a 2.4 meter-high by 1 meter wide poster board.
- ☐ The presentation must cover the same material as in the paper.
- ☐ Place the title of your paper and your paper number prominently at the top of the poster to allow viewers to identify your paper easily. Indicate 1) the paper's identification number, 2) title, and 3) authors' names.
- ☐ Highlight the authors' names, e-mail and address information in case the viewer is interested in contacting you for more information.
- ☐ You have complete freedom in displaying your information in figures, tables, text, photographs, etc in the poster.



- ☐ Include the background of your research followed by results and conclusions. A successful poster presentation depends on how well you convey information to an interested audience.

Set-up Your Poster

- ☐ Poster setup should be completed before 3:30 p.m. on November 5th.
- ☐ Please make sure that your paper number is clearly visible on your poster board.
- ☐ Presenters are required to be at their posters during their scheduled Open forum session.
- ☐ Tapes and other materials are available at the Information Desk, nearby the poster boards.

Remove Your Poster

Posters must be removed after the respective Open Forum sessions within half an hour.
Posters remaining after these times will be removed. WAI organizers will not be responsible for posters and materials left on poster boards after the stated hours.

Information Desk

Staff at the Information Desk will be available to assist you with location and other on-site needs. Tapes and scissors will be available for your use. If you have special needs for your poster presentation, please bring those supplies with you to the meeting.

PROGRAM OVERVIEW

Symposium Web: https://wai-emc.com/wai2026/

Symposium Hours

November 4, 2026, 8:30 – 17:30

November 5, 2026, 8:40 – 18:00

November 6, 2026, 8:30 – 12:00

November 4 – Wednesday

- ☐ Official Opening and Keynote Speeches
- ☐ Industry Plenary
- ☐ Technical Exhibition

November 5 – Thursday

- ☐ Industry Plenary
- ☐ Oral Sessions
- ☐ Best Student Paper Competition
- ☐ Poster Discussion
- ☐ Technical Exhibition
- ☐ Award Ceremony

November 6 – Friday

- ☐ Oral Sessions
- ☐ Technical Exhibition
- ☐ IBIS Summit China

2026 IEEE International Workshop on Advanced Interconnects
November 4-6, 2026

Date	Time	Agenda
Nov. 4th	08:30-09:00	**Opening Ceremony**
	09:00-12:00	**Keynote Speeches**
	12:00-13:40	**Lunch (Buffet)**
	14:00-15:30	**Industry Plenary**
	15:30-15:50	**Tea Break**
	15:50-17:30	**Industry Plenary**
	18:30	**Dinner (Buffet)**

2026 IEEE International Workshop on Advanced Interconnects
November 4-6, 2026

Date	Time	HUANYING Hall (环瀛厅)	HUIYUAN Hall (慧源厅)	YAXU Hall (雅叙厅)	YUQING Hall (玉清厅)	QIER Hall at Haining (Shuttle provided) (海宁圆正酒店启尔厅，杭州往返大巴接送)
Nov. 5th	8:40-10:20	*Industry Plenary*			*Best Student Paper Competition*	
	10:20-10:40	**Tea Break**				
	10:40-11:10	*Industry Plenary*			*Best Student Paper Competition*	
	11:10-12:00					
	12:00-13:30	**Lunch (Buffet) & Rest**				
	13:30-14:30	*[SS1] Electromagnetic Measurement and Near-Field-Based EMI Modeling*	*[SS2] Interconnect Reliability & Materials*	*Poster Session*	*Best Student Paper Competition*	*[SS3] Interconnect Characterization and Signal Integrity Analysis*
	14:30-15:10					
	15:10-15:30	**Tea Break**				
	15:30-16:15	*[SS4] Intelligent Parametric Modeling and Inverse Design of Microwave Components and Metasurfaces*	*[SS2] Interconnect Reliability & Materials*	*Poster Session*	*Best Student Paper Competition*	*Young Professionals Forum*
	16:20-16:30		*[SS5] Advanced Printed Circuit Technologies at Millimeter-wave and Terahertz Technologies*			
	16:30-17:00					
	17:00-18:00					
	18:30	**Banquet Dinner & Award Ceremony**				
Nov. 6th	8:30-9:30	*[SS6] Signal Integrity and Equalization for AI and High-Speed Links*	*[SS7] Electromagnetic Measurement and Testing of Components and Systems*	*[SS8] Advanced Computational Algorithms and Multiphysics Modeling for Integrated Systems*	*IBIS Summit China*	
	9:30-10:10			*[SS9] AI-Assisted TCAD and EDA for Devices and Circuits*		
	10:10-10:30					
	10:30-10:50	**Tea Break**				
	10:50-11:20	*[SS10] Power Integrity and EMI Protection for Power Delivery Networks*	*[SS11] Physics-Based Modeling and Design Optimization of Interconnects and Wireless Systems*	*[SS12] Advanced Multiphysics Analysis and Coupled-Physics Mechanisms*	*IBIS Summit China*	
	11:20-12:00					
	END					

KEYNOTE SPEECH I

TITLE	**Progress and Challenges in SI/PI with AI/ML**
TIME	9:00 – 09:40, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	James L. Drewniak



ABSTRACT

Artificial Intelligence LLMs and Machine Learning algorithms have had a profound impact on progress in many areas of signal integrity and power integrity. However, significant challenges still remain in providing solutions to everyday SI/PI design problems. High-bandwidth memory, facilitated by the thru silicon via (TSV), and rapidly shrinking silicon feature sizes using innovative lithography technologies have given rise to GPU and memory advances enabling this new age of AI/ML. Many innovations in SI/PI are underway using AI/ML for everything from facilitating the productivity of experienced engineers, to addressing some common and significant design challenges. Examples will be given showing the power of AI for dramatically enhancing the productivity of experienced engineers. Progress in applying ML to solve some of the most difficult and time-consuming problems in SI/PI will also be presented. Finally, thoughts and perspectives on AI/ML directions in SI/PI will be discussed.

BIOGRAPHY

James L. Drewniak (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana Champaign, IL, USA, in 1985, 1987, and 1991, respectively. He is currently a Curator's Professor Emeritus with the Missouri University of Science and Technology (Missouri S&T), Rolla, MO, USA. His research interests include electromagnetic compatibility, signal and power integrity, and electronic packaging.

KEYNOTE SPEECH II

TITLE	**High-Speed Cable Backplane Systems for AI Infrastructure: Speed of light Challenges at 224G and 448G**
TIME	9:40 – 10:20, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Stephen Scearce



ABSTRACT

As AI training and inference clusters scale to unprecedented bandwidth requirements, cable backplane interconnects have become a critical bottleneck and enabler for next-generation system architectures. This presentation examines the engineering challenges of designing, qualifying, and deploying high-speed cable backplane systems at 224 Gb/s and emerging 448 Gb/s data rates for AI infrastructure. Topics include signal integrity considerations for copper twinax cable at extreme data rates (including PAM4/PAM6 modulation schemes), mechanical float and connector design for reliable high-density interconnects, system BERT-based qualification methodologies, and lessons learned from large-scale cartridge reliability programs. The talk will address the tradeoffs between insertion loss, reach, and manufacturability that engineering teams must navigate as the industry pushes toward higher bandwidth per lane, and will share practical approaches to qualification and reliability testing that support high-volume deployment in AI data center environments.

BIOGRAPHY

Stephen Scearce is Senior Director of Cable Backplane Systems at Amphenol Communications Solutions, leading a global engineering organization responsible for the AI industry's high-speed cable backplane interconnects at 224G and 448G data rates. With over 25 years of experience in signal integrity, power integrity, mechanical/thermal design, and high-speed hardware systems, his career spans NASA, Cisco Systems, and now Amphenol. He holds a B.S. in Engineering Technology and an M.S. in Electrical Engineering, both Summa Cum Laude, from Old Dominion University, and holds multiple U.S. patents in signal and power integrity, EMC and Mechanical design. He is a longtime volunteer with the IEEE EMC Society, currently serving as Finance Vice President and previously as co-chair of the IEEE EMC+SIPI 2025 Symposium in Raleigh, NC.

KEYNOTE SPEECH III

TITLE	**High Bandwidth Memory and Computing-in-memory Technology**
TIME	10:40 – 11:20, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Cai Yimao



ABSTRACT

As large language models become more widely used, optimizing their deployment for AI applications on edge devices has drawn growing attention. Edge devices impose strict requirements on processing speed, energy use, and computational stability. Traditional von Neumann architectures, which mainly rely on DRAM and HBM, struggle to meet these demands in edge settings. This talk will explore a compute-in-memory strategy based on 3D VNAND Flash. It aims to overcome the VNAND Flash memory wall and enable more efficient deployment of large language models on edge devices.

BIOGRAPHY

Cai Yimao, Dean of the School of Integrated Circuits, Boya Distinguished Professor, doctoral supervisor, and Executive Director of the Innovation Center for Advanced Integrated Circuits at Peking University. He is a recipient of the National Outstanding Youth Science Fund, and the Special Government Allowance of the State Council. He has long been engaged in research on memory and AI chips. He has directed a number of national-level projects including the National Key R&D Program and Key Programs of the National Natural Science Foundation of China. He developed novel RRAM memory and in-memory computing intelligent chips with practical applications. He has published more than 150 papers in top-tier conferences and journals including IEDM, VLSI, and Nature Electronics, with over 100 authorized Chinese patents.

KEYNOTE SPEECH IV

TITLE	**Signal and Power Integrity of Advanced Semiconductor Packaging in the AI Era**
TIME	11:20 – 12:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Seungyoung Ahn



ABSTRACT

As Moore's Law slows down, advanced semiconductor packaging of 2.5D and 3D heterogeneous integration has emerged as the paramount driver for next generation performance and miniaturization. However, this dense architectural evolution introduces unprecedented challenges, making Signal Integrity (SI) and Power Integrity (PI) critical bottlenecks for high speed, reliable system such as High-Bandwidth Memory (HBM).

Addressing these complex multiphysics hurdles requires a paradigm shift in design methodologies. This talk explores the current landscape and future trajectory of advanced packaging technologies, emphasizing SI/PI design management is essential for system performance mentioning the revolutionary role of Machine Learning (ML) in reshaping package design. By leveraging AI-driven optimization and automated co-design, engineers can drastically reduce time-to-market and navigate vast design spaces efficiently. We would like to discuss how the synergy of advanced packaging and AI will shape the future of high-performance computing.

BIOGRAPHY

Seungyoung Ahn received the B.S., M.S., and Ph.D. degrees from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1998, 2000, and 2005, respectively, in electrical engineering. From 2005 to 2009, he was a Senior Engineer with Samsung Electronics, South Korea, where he was the in charge of high-speed board design for laptop computer systems. He is currently a Professor with the CCS Graduate School of Mobility, KAIST, Daejeon. He has been working in the area of signal and power integrity, wireless power transfer, and electromagnetic compatibility design publishing 300+ international conference and journal papers. He was the Distinguished Lecturer of IEEE EMC Society and the recipient of several awards including Technical Achievement Award 2024 and Motohisa Kanda Award 2021 in IEEE EMC society.

INDUSTRY PLENARY I

TITLE	**Advanced Packaging SI/PI Analysis: Challenges, Methodologies, and EDA Practices**
TIME	14:00 – 14:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Yin Sun, DetoolTech Ltd, China



ABSTRACT

Advanced packaging is rapidly evolving toward higher integration, higher bandwidth, and higher power density, while increasingly complex power delivery networks and high-speed interconnects are introducing new challenges for signal and power integrity. This presentation focuses on key SI/PI challenges in advanced packaging, covering analysis methodologies from DC power integrity and AC impedance to high-speed channel analysis. Through practical application cases, we will demonstrate how EDA technologies can support SI/PI analysis, problem diagnosis, and design optimization in advanced packaging.

BIOGRAPHY

Dr. Yin Sun has extensive experience in EDA technology development and product planning, with a focus on advanced packaging, signal integrity, and power integrity analysis. She has extensive practical experience in SI/PI simulation, modeling, and signoff. In recent years, she has focused on electrical integrity analysis for 2.5D/3D packaging, chiplet-based systems, and high-speed interconnects, with a commitment to developing domestic SI/PI analysis and verification solutions for advanced packaging.

INDUSTRY PLENARY II

TITLE	**AI-Driven Heterogeneous 3D IC Stacking: Redefining Advanced Packaging at the Chip Level** **AI 驱动 3D IC 异构异质堆叠，重构 3D IC 先进封装产业芯层级**
TIME	14:30 – 15:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Alex Zhao, Zhuhai Silicon Chip Technology Ltd., China



ABSTRACT

The continued evolution of AI computing is driving chip systems toward higher bandwidth, greater integration density, and increasingly sophisticated heterogeneous integration. In 3D IC systems, chiplets based on different functions, process nodes, and even technology platforms are integrated through high-density interconnects and vertical stacking, extending the design scope from individual dies to cross-die, cross-layer system-level co-design. This evolution introduces not only increasing challenges in interconnect density, power consumption, and thermal management, but also increasingly complex coupling across system architecture, physical implementation, multi-physics simulation, and process technology. Faced with an enormous design space and multiple competing objectives, conventional design methodologies based on point tools and sequential iterations are encountering growing limitations.

In this presentation, Dr. Zhao Yi, General Manager of Zhuhai Silicon Chip Technology Ltd. (SiChip), will explore a new “AI + 3D IC EDA” design paradigm and discuss how AI can enable system-level collaborative design for heterogeneous 3D integration. By building an innovative toolchain for 3D IC design,

key stages across the entire workflow—including architecture design, physical implementation, multi-physics simulation, verification, and testing—can be seamlessly connected.

The presentation will further introduce the collaborative deployment of SiChip's 3D IC EDA AI Agent, Chips Z, together with the 3Sheng EDA platform. By integrating advanced packaging know-how with AI capabilities, the solution enables cross-layer data collaboration, design space exploration, and automated multi-objective iterative optimization, continuously driving the convergence of an end-to-end closed-loop System-Technology Co-Optimization (STCO) workflow. Through AI-driven transformation of 3D IC design methodologies, toolchains, and collaborative workflows, advanced packaging can evolve from isolated point innovations toward system-level innovation, opening up new possibilities and a higher level of innovation for the 3D IC industry.

AI 算力持续演进，正在推动芯片系统向更高带宽、更高集成度和更复杂的异构异质集成发展。面向 3D IC，不同功能、不同工艺节点乃至不同技术体系的 Chiplet 通过高密度互连与立体堆叠形成复杂系统，设计对象也由单一芯片进一步延伸至跨 Die、跨层级的系统协同。随之而来的，不只是互连密度、功耗与热等问题的叠加，更是架构、物理设计、多物理场仿真、工艺等环节之间日益复杂的耦合关系。面对庞大的设计空间和多目标约束，依赖单点工具与串行迭代的传统设计方式正面临新的挑战。本次演讲，硅芯科技总经理赵毅博士将围绕“AI+3D IC EDA”新设计范式，探讨如何以 AI 驱动异构异质堆叠下的系统级协同设计。通过构建面向 3D IC 的创新型工具链，贯通架构设计、物理实现、多物理场仿真、验证及测试等全流程关键环节。并通过硅芯科技 3D IC EDA AI Agent——Chips Z 及 3Sheng EDA 工具平台的协同实践，进一步融合先进封装 Know-how 与 AI 能力，实现跨层级数据协同、设计空间探索以及多目标自动迭代寻优，推动端到端 STCO 闭环持续收敛。以 AI 重塑 3D IC 设计方法、工具体系与协同流程，推动先进封装从单环节创新走向系统级创新，进一步打开 3D IC 产业新的“芯层级”。

BIOGRAPHY

Holding a Ph.D. from the University of Southampton, UK, under the supervision of Royal Society Fellow Professor Bashir Hashimi, he embarked on 2.5D/3D stacked IC design research in 2008 as part of one of the world's earliest pioneering research teams exploring advanced chip architecture methodologies, having collaborated with IMEC for 3D-IC technology validation. With 15 years of dedicated R&D in 3D integrated circuit design, he has published several excellent papers and awarded the VLSI-SOC Best Paper.

Currently serving as Founder and Chief Scientist at Zhuhai Silicon Chip Technology Ltd. , he has been a majority of leading national research initiatives. He directs the team in developing self-proprietary 2.5D/3D Stacked IC EDA tools, enabling critical advancements in the semiconductor industry through backend full-flow EDA tools and solutions.

英国南安普顿大学博士，师从英国皇家科学院院士（Prof Bashir Hashimi），2008 年投身 2.5D/3D 堆叠芯片设计研究，是当时世界最早期研究前沿芯片架构设计方法的研究团队之一，与 IMEC 完成 3D-IC 成果验证。深耕三维集成电路设计研发 15 年，发表多篇国际顶尖论文并获 VLSI-SOC 国际最佳论文。

现任珠海硅芯科技有限公司的创始人兼首席科学家，承担国家重点研发计划项目，带领团队自研 2.5D/3D 堆叠芯片 EDA 软件，以后端全流程 EDA 工具及解决方案推动芯片产业实现关键技术突破。

INDUSTRY PLENARY III

TITLE	**From Wafer to System: Advanced Packaging Solutions for Heterogenous Integration and Chiplets**
TIME	15:00 – 15:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Boping Wu, JCET Group Co., China



ABSTRACT

The end of conventional Dennard scaling and the rising cost of advanced node lithography have driven the semiconductor industry toward a paradigm shift: from monolithic System-on-Chip (SoC) to heterogeneous integration and chiplet-based architectures. This transition, however, places extreme demands on nanoscale fabrication, interfacial reliability, and system-level thermal-mechanical management—demands that cannot be met by traditional back-end packaging alone. In this talk, we present a comprehensive advanced packaging roadmap spanning from 2.5D interposer technologies to full 3D stacked systems, with an emphasis on the underlying nano-packaging science and manufacturing innovation.

We examine the technological landscape of 2.5D and 3D packaging solutions, comparing silicon interposers, organic interposers, and emerging bridge-die architectures in terms of electrical performance, thermal management, and cost efficiency. Particular emphasis is placed on through-silicon via (TSV) and through-glass via (TGV) technologies as critical enablers for vertical integration, addressing challenges in aspect ratio control, void-free filling, and reliability under thermal cycling.

A core contribution involves cross-scale thermomechanical modeling methodologies that bridge sub-micron structural mechanics with wafer-level warpage analysis. These finite element-based simulations enable predictive assessment of stress distributions in complex multi-material stacks, informing design rules for high-density interconnects.

To address the process complexity of conformal dielectric deposition in TSV/TGV structures, we introduce an AI+EDA co-optimization framework. Specifically, machine learning models are trained to predict and control ALD and CVD process parameters, reducing development cycles for ultra-thin barrier and seed layers critical for advanced packaging metallization. Experimental validation on a pilot line demonstrates that AI-optimized ALD reduces defect density by two orders of magnitude compared to conventional recipe-based approaches.

Finally, we discuss the integration roadmap toward full 3D chiplet stacking with nano-scale interconnects and emerging thermal interface materials. The talk concludes with a perspective on standardization needs (UCIe, BoW) and the role of nano-packaging in enabling domain-specific accelerators for AI, HPC, and photonic computing.

BIOGRAPHY

Dr. Boping Wu earned his Ph.D. in Electrical Engineering from the University of Washington, Seattle. He is currently Vice President of JCET Group and General Manager of the Technology Service Business Unit. Dr. Wu is an inventor on dozens of patents and author of numerous refereed publications on 3-D system integration and high speed interconnects. Over a 20-year career, he has led packaging R&D and product prototyping programs at various semiconductor companies, such as Philips, IBM, and Intel.

INDUSTRY PLENARY IV

TITLE	**Data Storage Innovations & Trends**
TIME	16:00 – 16:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Jianjun LUO, Hangzhou Dianzi University, China



ABSTRACT

Solid-State Drive (SSD) is rising to replace traditional hard drive (HDD) and flash memory becomes the most popular Non-Volatile memory in data storage industry. Supercomputing and AI demands greatly stimulated the storage technology development. It is facing challenge of higher density and performance as well as reliability when going to the next generation with the most advanced semiconductor process. Flash memory controller should take actions to clean the issues for the next generation Solid-State Drive with Flash Memory. At the same time, new memory devices, such as RRAM, MRAM and FeRAM, are exploring their niche market. However, these new memory technologies have to make trade-off to satisfy the unique applications. This key-note speech is going to allocate these memory devices in dedicated applications according to their advantages and disadvantages.

BIOGRAPHY

Jianjun (Jerome) Luo, the Dean of Microelectronic Research Institute in Hangzhou Dianzi University, also the founder and CTO of Sage Microelectronics. He earned a PhD in semiconductor material from Zhejiang University in China, a Master's in Microelectronics from the Hangzhou Dianzi University, and a Bachelor's in Electronics Engineering from Shanghai Jiaotong University. He founded Baleen Systems Inc in Silicon Valley in USA and started his new venture of Sage Micro in China since 2011, accumulated his experience in communication and storage IC design for more than 30 years. He won the 2nd Prize of National Scientific and Technological Progress Award, and Ho Leung Ho Lee Foundation's Scientific and Technological Award.

INDUSTRY PLENARY V

TITLE	**High-Speed Link Analysis Across Electrical and Optical Domains: Co-Simulation and Testing**
TIME	16:30 – 17:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Sun Anbing, Ruijie Networks, China



ABSTRACT

Growing bandwidth demand continues to push data rates higher. As a result, electrical channels face shorter practical reach and tighter design margins, driving wider use of optical links in high-speed systems. Retimed pluggables, LPO, NPO, and CPO represent different approaches to optical connectivity, each placing the boundary between the electrical and optical domains at a different point. The degree of separation between the two domains determines whether their impairments can be evaluated independently or must be considered at the system level. Drawing on a 112G application case, the presentation explores system-level electro-optic co-simulation and test design, including correlation between simulation and measurement, link budget allocation, and practical SI considerations. Beyond simulation and testing, the presentation discusses how signal integrity and optical engineering teams can combine system-level understanding with practical experience to guide system design and architecture decisions while methods and standards continue to evolve.

BIOGRAPHY

Sun Anbing is a senior hardware system engineer at Ruijie Networks. He joined ZTE in 2009, focusing on research in signal integrity / power integrity and having 16 years of experience in high speed core switch device development. He joined Ruijie Networks in 2020 and currently serves as a hardware system architecture engineer, leading the hardware system architecture design of next generation data center switches and research on new technologies.

INDUSTRY PLENARY VI

TITLE	**Interconnection & Simulation Techniques for Next-Generation NPO Switch**
TIME	17:00 – 17:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Rongyao Tang, FiberHome Telecommunication Technologies Co., Ltd, China



ABSTRACT

AI scale-up computing has driven the interconnect bottleneck off the die and onto in-cabinet channels, making copper-based electrical links impractical as lane rates move toward 200G. Near-package optics (NPO) offers a pragmatic engineering balance, capturing most of the signal-integrity benefits of co-packaged optics while preserving repairability and a conventional supply chain. This work presents a 51.2T NPO switch integrating sixteen 32×100G/3.2T optical engines, detailing flip-chip packaging, multi-physics system-technology co-optimization (STCO), and calibrated electrical-optical-electrical end-to-end simulation validated against hardware. We further discuss scalability to 6.4T/12.8T through advanced packaging and co-simulation.

BIOGRAPHY

Tang is the Staff Engineer and Interconnect Chief Expert at FiberHome, leading signal-integrity design of high-speed electro-optical channels in packages and PCBs, backed by 10+ years in high-speed design and an HUST optical/electronic background.

INDUSTRY PLENARY VII

TITLE	**Photonic Components and Packaging Technologies for Optical Interconnects**
TIME	8:40 – 9:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Torsten WipiejewskiJob, Huawei Technologies Duesseldorf GmbHMunich, Germany

ABSTRACT
TBD

BIOGRAPHY
Dr. Torsten Wipiejewski joined Huawei Technologies in 2014 and is responsible for the European technology sourcing of Huawei's Hardware Engineering Institute. His interest covers all hardware aspects for products ranging from smart watches to optical communication systems. Previously, Torsten was an investor in renewable energy, CEO at Optogan (Germany, Finland) making blue LEDs, and COO at Firecomms (Ireland) making optical transceivers for automotive and home networking applications. He also held management positions at ASTRI in Hong Kong, Agility Communications in Santa Barbara, CA, USA as well as Infineon, Osram, and Siemens in Germany. Torsten received a "summa cum laude" Ph.D. degree in electrical engineering from the University of Ulm, Germany and has been an executive member of several international conferences. He was the General Chair of ECTC2008 and has lectured several courses at conferences and universities. He holds more than 30 patents and has published over 100 scientific papers and presentations.

INDUSTRY PLENARY VIII

TITLE	**Emerging Trends and Challenges: System-Level Signal Integrity and Power Integrity/Delivery in the AI/SI Superchip Era**
TIME	09:10 – 09:40, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Kinger Cai, Arm Limited, USA



ABSTRACT
The rapid evolution of AI toward superintelligence is driving unprecedented growth in computing performance, memory bandwidth and capacity, high-speed interconnects, and power density. These trends introduce increasingly complex challenges in signal integrity (SI), power integrity (PI), power delivery, and thermal management across next-generation AI supercomputing platforms.
This presentation explores emerging architectures, including NVIDIA Vera Rubin and AMD Helios, and the evolution of memory technologies such as DDR, LPDDR, MRDIMM, SOCAMM, and HBM, alongside high-speed interconnects including PCIe, CXL, NVLink, UALink, and Ethernet. Key SI/PI challenges include channel loss, crosstalk, jitter, simultaneous switching noise, PDN impedance, voltage transients, and complex 3D packaging and interconnects.
The presentation highlights opportunities in advanced electromagnetic modeling, channel equalization, integrated system-level SI/PI co-design, optimized power delivery, liquid cooling, and comprehensive validation. It emphasizes that compute, memory, interconnects, power delivery, and thermal management must evolve together to enable scalable, energy-efficient, and reliable AI supercomputing infrastructure.

BIOGRAPHY
Kinger is Sr. Principal / Director driving Super AI platform electrical architecture design validation, & HVM, and advancing industry Power & Signal Integrity standards, in ARM.
Kinger was a Principal Engineer/Director in Intel, led cross-functional teams in AI PC coherent architecture strategies across CPU / GPU platforms and oversaw numerous SoC design & sign-off across mobile, client, discrete GPU, & CPU server products.

Kinger earned his Ph. D from Shanghai Jiao Tong University in 2001 and MBA degree from W.P. Carey business school in ASU in 2008.
Kinger is an IEEE Sr. Member, currently serves as Vice Chair in IBIS Open Forum.
Kinger has been focusing on signal & power integrity domains for 25+ years.
Kinger holds 14 granted patents, and published 30+ papers.

INDUSTRY PLENARY IX

TITLE	**M3EM Studio: High-Performance Electromagnetic Simulation for System-Level EMC/EMI Analysis**
TIME	09:40 – 10:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Li Xiang, Third Paradigm (Ningbo) Technology Co., Ltd. China



ABSTRACT
System-level electromagnetic compatibility (EMC) and electromagnetic interference (EMI) analysis requires efficient modeling of complex geometries and interactions between electromagnetic fields and circuits. This presentation introduces M3EM Studio, a high-performance electromagnetic simulation platform combining the time-domain finite integration technique (FIT), Advanced Conformal Enhancement (ACE) technology, and GPU acceleration. ACE improves the representation of geometric details and curved boundaries, while GPU acceleration enables efficient full-wave simulation of large-scale models. Synchronous and asynchronous field – circuit co-simulation supports the coupled analysis of electromagnetic structures and circuit responses. Complementary macromodeling tools provide passivity, causality, and reciprocity assessment and correction, together with SPICE model generation for system-level simulation. Integrated preprocessing, postprocessing, and workflow automation support various applications. The presentation outlines the platform's numerical methods and computational capabilities, with an emphasis on electromagnetic coupling, interference assessment, and EMC-oriented design.

BIOGRAPHY
Li Xiang is currently the Product Director at Third Paradigm (Ningbo) Technology Co., Ltd., where he leads the product definition of M3EM Studio, a GPU-accelerated full-wave electromagnetic simulation software for system-level EMC/EMI analysis. He has nearly a decade of industry experience spanning EMC simulation, device modeling, and IC design. Prior to joining Third Paradigm, he was an EMC Expert at Huawei, where he was deeply involved in the EMC design of several best-selling digital products, and later worked at Nano Core Chip (NCC), a Hangzhou-based AI chip company, where he led on-chip ESD protection design for multiple mass-production ICs. He received the Master's degree from Zhejiang University, Hangzhou, China, in 2018.

INDUSTRY PLENARY X

TITLE	**Next-Generation Modular Ethernet Switches: Challenges and Trade-offs in High-Speed Internal Interconnects**
TIME	10:40 – 11:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Siyuan Yang, Cisco, China



ABSTRACT

This presentation explores the critical demands of AI data centers on modular Ethernet switches and their high-speed internal interconnects. Driven by rapidly increasing bandwidth requirements, modern switches face major complexities, including large chip packaging, ultra-high power consumption, and high-speed SerDes that make internal interconnect design highly challenging. Using a comparative case study of major Cisco switching platforms, this session delivers a clear analysis of PCB backplanes, direct orthogonal connections, and cable backplanes across key trade-offs: channel loss, cost, reliability, and serviceability. Ultimately, this talk provides practical architectural frameworks and engineering insights to guide the reliable design of next-generation switching systems.

BIOGRAPHY

Siyuan Yang is a Principal Engineer and Hardware R&D Manager at the Cisco China Research and Development Center. In this dual leadership role, he manages the hardware engineering team for enterprise core switches while simultaneously directing the architecture design for Cisco's next-generation modular platforms. With over 20 years of deep industry expertise, he has successfully delivered numerous enterprise modular switches and some AI data center switching platforms. He graduated with a Master’s degree from Beihang University (BUAA) in 2003.

OVERVIEW OF BEST STUDENT PAPER COMPETITION

VENUE	YUQING Hall (玉清厅)
TIME	8:40-16:30 November 5th
FINALISTS	
8:40-8:55	**No.1 A 0.1-0.84 GHz Bandpass Filter with Reconfigurable Frequency, Bandwidth and Multiple Transmission Zeros (#1571354398)** *Xu Zhu (National Key Laboratory of Electromagnetic Space Cognition Technology, China)*
8:55-9:10	**No.2 A Hybrid PEEC-FEM Framework for Two-Way Electrothermal Analysis of Planar Transformers (#1571350995)** *Hangkai Zhang (Zhejiang University); Xu Wang (DeTooLIC Technology Co., China); Bo Pu and Yanwu Wang (DeTooLIC Ltd. Technology, China); Xinglin Sun (Zhejiang University, China)*
9:10-9:25	**No.3 A General Peeling Algorithm Based on Conductor and Dielectric Losses Compensation for Impedance Reconstruction (#1571353594)** *Jiyang Liu, Zi-Xi Chen, Si-Yao Tang and Xing-Chang Wei (Zhejiang University, China)*
9:25-9:40	**No.4 Pre-Layout Case Study of Lateral and Vertical Power Delivery Using PDN Shape Synthesis (#1571345363)** *Ruiqi Dai, Haran Manoharan and Suho Lee (Missouri University of Science and Technology, USA); Kundan Chand and Grace Yu (Meta Platforms, USA); Chulsoon Hwang (Missouri University of Science and Technology, USA)*
9:40-9:55	**No.5 Quantum-Kernel Residual Regression for Metal Contacts to β-Ga2O3 (#1571354187)** *Qi Shen, Jintang Wang, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)*
9:55-10:10	**No.6 Agent-Guided Iterative Signal-Integrity Design: PCIe 6.0 and DDR5 Case Studies (#1571357515)** *Qiuhong Ye, Jienan Chen and Kuo Liao (University of Electronic Science and Technology of China, China)*
10:40-10:55	**No.7 Signal Integrity Analysis of Narrowband near-Field Communication Links Based on Low-Frequency Magnetoelectric Mechanical Antennas (#1571356416)** *Shizhan Jiang (Chongqing University, China); Ruixin Xu (Chongqing university, China); Wei Zhou (Chongqing University, China); Zhaoqiang Chu (Harbin Engineering University, China); Da Yi and Ming-Chun Tang (Chongqing University, China)*
10:55-11:10	**No.8 Multiharmonic Spatiotemporal Modulation for Crosstalk Control in Coupled Transmission Lines (#1571353809)** *Kishwar Ali (University of Aquila, Italy); Ayesha Shabbir, Giulio Antonini and Daniele Romano (University of L'Aquila, Italy); Martin Štumpf (VUT, Czech Republic); Elia Mattucci and Petr Kadlec (Brno University of Technology, Czech Republic); Francesco Ferranti (Luleå University of Technology, Sweden); Jonas Ekman (Lulea University of Technology, Sweden)*
11:10-11:25	**No.9 Efficient via Placement Optimization for Irregular Power Distribution Network Using Deep Reinforcement Learning (#1571365891)** *Junjie Ren, Ling Zhang, Li Jiang, Keyi Ding, Chenxu Zhang and Er-Ping Li (Zhejiang University, China)*
11:25-11:40	**No.10 Real-Time Dynamic Magnetic Hysteresis Compensation in TMR Sensors Using Point-by-Point Inverse PI Model (#1571350699)** *Tianhao Pan, Jun Wang and Xing-Chang Wei (Zhejiang University, China)*

11:40-11:55	**No.11 Three-Dimensional SAR Reconstruction from Two-Plane Electric-Field Measurements Using Numerical Green's Functions (#1571355763)** *Zhelun Chen and Xing-Chang Wei (Zhejiang University, China)*
13:30-13:45	**No.12 Macrobending Loss in Single-Mode Fibers: Comparison of Analytical and Full-Vector Finite-Element Models (#1571347175)** *Zanyu Xu and Xing-Chang Wei (Zhejiang University, China)*
13:45-14:00	**No.13 Construction of a Repeatable 6G-Oriented Channel Model in a Reverberation Chamber (#1571353916)** *Boyan Zhang, Tian Zhou, Sen Zhang and Yuan Zhao (Chengdu University of Information Technology, China)*
14:00-14:15	**No.14 A Hybrid Finite Element Physics-Informed Neural Network Framework for Electromagnetic-Thermal Analysis (#1571354929)** *Qingnan Fan, Yijie He and Huan Huan Zhang (Xidian University, China)*
14:15-14:30	**No.15 Inductance Modeling of Inclined Bond Wires with Finite Length and Return Path Effects (#1571351112)** *Xiaoya Zhou (Beijing University of Posts and Telecommunications, China); Dan Shi (Beijing University of Posts and Telecommunications, China); Yanchi Liu (Beijing University of Posts and Telecommunications, China); Peng Zhang (State Radio Regulation Committee, China); Jinde Wang and Machen Yin (Beijing University of Posts and Telecommunications, China)*
14:40-14:55	**No.16 Stacking-Dependent Dipole Engineering of Metal/β-Ga2O3 Contacts with Atomically Thin h-BN Interlayers (#1571353696)** *Tianyu Lin and Wenjie Yin (National University of Defense Technology, China); Zhiqiang Fan (Changsha University of Science and Technology, China); Yuxiong Long and Jiayu Dai (National University of Defense Technology, China)*
14:55-15:10	**No.17 A qNEHVI-Based Bayesian Optimization Framework for Ku-Band Hairpin Filter Design (#1571353429)** *Yuhao Pan, Junhan Huang and Liang Chen (Shanghai University, China)*
15:30-15:45	**No.18 A Physics-Driven Deep Finite Element Method for Fast Electro-Thermal Analysis of 3D Interconnects (#1571345974)** *Yijie He, Qingnan Fan, Huan Huan Zhang, Bian Wu and Ying Liu (Xidian University, China)*
15:45-16:00	**No.19 An Absorption Spectrum is Not a Thermometer (#1571365587)** *Kun-Lai Li (Beihang University); Weikang Si (National Institute of Metrology, China); Rui-Yun Liu, Zhengpeng Wang, Yongjun Xie, Tao Zhang and Xiangxuan Feng (Beihang University, China)*
16:00-16:15	**No.20 Per-Frequency Relative-Gain Self-Calibration for Sequential Sphere-Scan Quiet-Zone Reconstruction (#1571365646)** *Rui-Yun Liu and Zhiping Li (Beihang University, China); Kun-Lai Li (Beijing University of Aeronautics and Astronautics, China); Weikang Si (National Institute of Metrology, China)*
16:15-16:30	**No.21 A Wideband Hollow Rectangular Dielectric Waveguide Antenna for Sub-THz Wireless Interconnect Applications (#1571358228)** *Changsheng Sun and Xiaochun Li (Shanghai Jiao Tong University, China); Haibing Zhan (Hunan Institute of Engineering, China); Ken Ning (Shenzhen University, China)*

OVERVIEW OF SESSION I

SESSION	SS1 Electromagnetic Measurement and Near-Field-Based EMI Modeling
VENUE	HUANYING Hall (环瀛厅)
TIME	13:30-15:00 November 5th
SESSION CHAIRS	Da Yi, Chongqing University Pei Xiao, Hunan University Xing-Chang Wei, Zhejiang University
TECHNICAL TALKS	
13:30-13:45	**The Development Trend of Electromagnetic Safety in Integrated Circuits (#1571348874)** *Zhaowen Yan, Jianhao Ge, Fuyu Zhao and Siyuan Ma (Beihang University, China)*
13:45-14:00	**Reflection Loss of an EM Absorber from One-Port and Two-Port Free-Space Measurements (#1571345783)** *Branimir Pejcinovic and Ha Tran (Portland State University, USA); Adithya S. Ramachandran, Kent Thompson and Robert L. Doneker (TangiTek, LLC, USA)*
14:00-14:15	**Electromagnetic Interference Characterization of Integrated Circuits Based on near-Field Scanning and Dipole Reconstruction Techniques (#1571347798)** *Han Dong-Hao and Xing-Chang Wei (Zhejiang University, China)*
14:15-14:30	**New Fast System-Level EMI Simulation Method - Reverberant and Direct Field (#1571353960)** *Weitao Dai and Paul Bremner (RobustPhysics, USA)*
14:30-14:45	**Co-Simulation of Electromagnetic Fields and Cable Networks for Signal Integrity in Noisy Environments (#1571353963)** *Weitao Dai and Paul Bremner (RobustPhysics, USA)*
14:45-15:00	**Radial-Loaded Concentric-Arc Planar Sensor for Partial Discharge Detection: 1.5-3 GHz Receiving- Response Simulation (#1571360315)** *Jiyang Zhang, Pei Xiao and Gaosheng Li (Hunan University, China)*

OVERVIEW OF SESSION II

SESSION	SS2 Interconnect Reliability & Materials
VENUE	HUIYUAN Hall (慧源厅)
TIME	13:30-16:00 November 5th
SESSION CHAIRS	Haohui Long, Shanghai Jiao Tong University Yunwen Wu, Shanghai Jiao Tong University
TECHNICAL TALKS	
13:30-13:50	**Interconnection Mechanisms and Electromigration Reliability of Nanotwinned Copper Pillars for Advanced Packaging (Invited)** *Dr. Zicheng Sa (Harbin Institute of Technology, China)*
13:50-14:10	**Low-Temperature, Low-Pressure Cu-Cu Bonding Using Perpendicular Nanotwinned Copper (Invited)** *Dr. Zihao Xiang (Shanghai Jiao Tong University, China)*
14:10-14:30	**Reliability simulation and modeling for advance package processing (Invited)** *Dr. Zhang Shi (IC Research Technology (WuHan) Co. LTD, China)*
14:30-14:50	**Reliability Study on Flexible Glass and Glass-Based Packaging Technology (Invited)** *Dr. Yang JinFa (TriumphScience&Technology Flexible Display Materials Co., Ltd., China)*
14:50-15:10	**Fine Pitch RDL Interconnection on Glass Substrates: Materials, Interfaces, and Reliability (Invited)** *Wei Koh (Pacrim Technology, USA)*
15:30-15:45	**Study on Process Control of Low-Temperature, Low-Pressure Cu-Cu Bonding Using Perpendicular Nanotwinned Copper (#1571371211)** *Zihao Xiang (Shanghai Jiaotong University, China); Xingya Pan and Haohui Long (Shanghai Jiao Tong University, China); Xiaoqin Zeng and Yunwen Wu (Shanghai Jiaotong University, China)*
15:45-16:00	**Transient in-Plane Temperature Nonuniformity and Microbump Defects During Thermocompression Bonding of Multi-Chiplet Packaging (#1571359625)** *Wang Hexin (Central South University, China); Yiou Qiu (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Zimeng Guo (Central South University, China); Zhen Liu and Qiaobo Dai (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Chen Zhuo and Wenhui Zhu (Central South University, China)*

OVERVIEW OF SESSION III

SESSION	SS3 Interconnect Characterization and Signal Integrity Analysis
VENUE	**Venue: Qier Hall, Haining Yuanzheng Hotel** **Round-trip shuttle service will be provided. The shuttle will depart from the Hangzhou Blossom Water Museum Hotel at approximately 12:30 PM on November 5, after lunch, and return to Hangzhou after the session for the conference banquet that evening.** **地点：海宁圆正酒店启尔厅** **会议提供往返大巴接送。大巴将于 11 月 5 日午餐后约 12:30 从杭州宝盛水博园大酒店出发，活动结束后返回杭州，参加当晚的大会晚宴。**
TIME	13:30-14:45 November 5th
SESSION CHAIRS	Ping Li, University of Electronic Science and Technology of China Xiaochun Li, Shanghai Jiao Tong University Min Tang, Shanghai Jiao Tong University
TECHNICAL TALKS	
13:30-13:45	**Double-Sides Launch Point Impedance Drift Correction for Accurate PCB Characteristic Impedance Measurement (#1571323552)** *Wai Hong Chee (Keysight Technologies, Inc., Malaysia); Brian Chi (Keysight Technologies, Taiwan); Eason Yang (Keysight Technologies, Inc., Taiwan)*
13:45-14:00	**Design and Tolerance Analysis of Differential Transmission Structures for High Speed Connectors (#1571367249)** *Lei Deng (LinkE Technologies, China); Lidong Cai (New H3C Technologies Ltd., China); Licheng Li (New H3C Technologies Ltd, China); Chaoqiang Zang (HUNAN University, China); Yinzhu Tang (Southwest University of Science and Technology, China); Chi Lidong (Hunan University, China); Yihong Qi (unknown)*
14:00-14:15	**Decomposition of Far-End Crosstalk in a Memory Channel (#1571364440)** *Wenzhi Wang and Qihang Shang (DeTooLIC Ltd. Technology, China)*
14:15-14:30	**UCIe Link Compliance Analysis in a Multi-Functional S-Parameter Post-Processing Platform (#1571364857)** *Zhifei Xu and Yajun Chen (DeTooLIC Ltd. Technology, China)*
14:30-14:45	**A Harmonic-Domain Electrical Modeling Framework for EMC and SI/PI Analysis (#1571347048)** *Alessandro Sona and Federico Tramarin (University of Padova, Italy)*

OVERVIEW OF SESSION IV

SESSION	SS4 Intelligent Parametric Modeling and Inverse Design of Microwave Components and Metasurfaces
VENUE	HUANYING Hall (环瀛厅)
TIME	15:30-17:05 November 5th
SESSION CHAIRS	Jianan Zhang, Southeast University Feng Feng, Tianjin University Meng Meng Li, Nanjing University of Science and Technology
TECHNICAL TALKS	
15:30-15:50	**Physics-Guided Learning for Advanced 3D Packaging: From Thermal Simulation to Stress Prediction (Invited)** *Zhou Jin (Zhejiang University, China)*
15:50-16:05	**A Hybrid Physics-Machine Learning Framework for Data-Efficient and Scalable Parametric Modeling of Frequency-Selective Rasorbers (#1571358634)** *Meng Yuan Li and Jianan Zhang (Southeast University, China)*
16:05-16:20	**Data-Efficient Multiphysics Parametric Modeling of Frequency Selective Surfaces via Physics-Inspired Iterative Framework (#1571359190)** *Liaoyuan Xu and Jianan Zhang (Southeast University, China)*
16:20-16:35	**Conditional Diffusion-Based Inverse Design of Pixelated Metasurface Absorbers (#1571357809)** *Niting Mao and Jianan Zhang (Southeast University, China)*
16:35-16:50	**Gradient-Based Optimization for Rapid Beamforming of Coding Metasurfaces via Differentiable Quantization (#1571357550)** *Ziyi Zhang and Jianan Zhang (Southeast University, China)*
16:50-17:05	**Efficient Inverse Design of Metasurfaces for Multidimensional Electromagnetic Wave Control via Adjoint Sensitivity Based on the Discrete Dipole Approximation (#1571359212)** *Hao Li and Jianan Zhang (Southeast University, China)*

OVERVIEW OF SESSION V

SESSION	SS5 Advanced Printed Circuit Technologies at Millimeter-wave and Terahertz Technologies
VENUE	HUIYUAN Hall (慧源厅)
TIME	16:05-17:15 November 5th
SESSION CHAIRS	Yifei Zhang, Shandong University Weihong Liu, Xi'an University of Posts and Telecommunications
TECHNICAL TALKS	
16:05-16:25	**60-93.5 GHz Broadband Bond Wire Compensation Technique Based on DGS (#1571365689 Invited)** *Wei Hong Liu (Xi'an University of Posts & Telecommunications, China); Lei Zhou (XUPT, China)*
16:25-16:45	**Oxide Semiconductor Based Tunable Devices at Millimeter-Wave and Terahertz Frequencies (#1571353902 Invited)** *Yifei Zhang (Shandong University, China)*
16:45-17:00	**Study on Time Domain Reflectometry (TDR) Impedance Curve Characteristics (#1571353915)** *Victor Qi (AKMMV, China)*
17:00-17:15	**Heterogeneous Polymer Integration for High-Frequency Interconnects in Advanced Packaging Applications (#1571353745)** *Jian Song and Lei Chen (Shandong University, China); Tian Hao Ling (Aerospace Information Technology University, China); Yifei Zhang (Shandong University, China)*

OVERVIEW OF SESSION VI

SESSION	SS6 Signal Integrity and Equalization for AI and High-Speed Links
VENUE	HUANYING Hall (环瀛厅)
TIME	8:30-10:20 November 6th
SESSION CHAIRS	Shufang Li, Beijing University of Posts and Telecommunications Xiaohe Chen, China University of Petroleum (Beijing) Fayu Wan, Nanjing University of Information Science and Technology
TECHNICAL TALKS	
8:30-8:45	**Intra-Pair Skew Modeling and Budgeting for Ethernet Based AI Rack Design (#1571347368)** *Yang Wu (Intel Corporation, China); Xinjun Zhang (Intel Asia-Pacific Research & Development Ltd., China); Weizhe Li (Intel Corp., China); Yinglei Ren (Intel Asia-Pacific Research & Development Ltd., China)*
8:45-9:00	**Impact of Fiber-Weave Effects on Differential Skew and PAM4 Eye Performance in High-Speed Interconnects (#1571353288)** *Yan Li (Cisco Systems, Inc., China); Felen Fu (Cisco Systems, Inc, China); Kai Li (Cisco Systems, Inc., China); Xiao-Ding Cai and Bidyut Sen (Cisco Systems, Inc, USA)*
9:00-9:15	**Bandwidth vs. Loss Trade-off for PAM-n Modulations Toward 400 Gbps Data-Rates (#1571353293)** *Francesco de Paulis (University of L'Aquila, Italy); Sherman Shan Chen (Apple UK, USA); Tim Wang Lee and Mike Resso (Keysight Technologies, USA)*
9:20-9:35	**Link-Aware Distributed Negative-Group-Delay Phase Equalization for 112-Gb/s PAM4 Links (#1571353338)** *Xiang Fang and Fayu Wan (Nanjing University of Information Science and Technology, China); Blaise Ravelo (NUIST, China); Hongchuan Jia (Nanjing University of Information Science and Technology, China); Sébastien Lallechère (Université Bourgogne Europe & AFSCET, France)*
9:35-9:50	**Quad-Band Negative Group Delay Circuit for Inter Symbol Interference Suppression (#1571353575)** *Hongchuan Jia and Fayu Wan (Nanjing University of Information Science and Technology, China); Xiaohe Chen (China University of Petroleum, China); Blaise Ravelo (NUIST, China); Sébastien Lallechère (Université Bourgogne Europe & AFSCET, France)*
9:50-10:05	**Signal Integrity Analysis Framework and Design Optimization for PCIe 7.0 Interconnects (#1571358674)** *Harrison Xue (Lenovo, China); Boby Yan (Lenovo, USA); Zuli Qin and Zixiang Zhou (Cadence, USA); Yanwu Wang (DeTooLIC Ltd. Technology, China)*
10:05-10:20	**Signal Integrity Challenges of Rack-Scale CXL Memory Pooling Solution (#1571358828)** *Harrison Xue and Richard Li (Lenovo, China); Jiang Zhu and Jingwen Luo (Signal Easy, China); Yanwu Wang (DeTooLIC Ltd. Technology, China)*

OVERVIEW OF SESSION VII

SESSION	SS7 Electromagnetic Measurement and Testing of Components and Systems
VENUE	HUIYUAN Hall (慧源厅)
TIME	8:30-10:25 November 6th
SESSION CHAIRS	Ge Shi, China Jiliang University Yan Li, China Jiliang University Zhipeng Xu, China Jiliang University Zhao Yuan, Chengdu University of Information Technology
TECHNICAL TALKS	
8:30-8:50	**Novel EMC Test Methods for Automotive-Grade Integrated Circuits (Invited)** **车规级集成电路电磁兼容测试新方法研究** *Jianfei Wu (Tianjin Institute of Advanced Technology, China)*
8:50-9:10	**Quantized Optical Lattice Constant-Based Nanometrology and Its Applications (Invited)** **量子化光晶格常数纳米计量技术与应用** *Xiao Deng (Tongji University, China)*
9:10-9:25	**A Novel ESD Test Platform for Electrode Moving Speed Effect Investigation (#1571346964)** *Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Yang Meng (China Academy of Science, China); Fang Wang, Xiaoye Fu and Wenli Wang (Guizhou Normal University, China); Yan li Chen (Tibet University, China)*
9:25-9:40	**TVS Harmonic Performance Evaluation with Communication Protocol Signals** *(#1571352631)* *Jingkun Mao (Tianjin University of Technology, China); John Xiao (Keysight, China & Keysight (China), China); Xiaohe Chen (China University of Petroleum, China)*
9:40-9:55	**Beyond the 10 dB Assumption: An Investigation of 3 m and 10 m Radiated Emission Measurements (#1571346009)** *Mayur Yeola (Automotive Research Association of India, India); Abhijit Mulay (ARAI, India)*
9:55-10:10	**Validation of the Temporal Correspondence Between Microcontroller Loop-Program Execution Timing and Electromagnetic Emissions (#1571353921)** *Kaipeng Yang, Junjie Wang, Yong Zhou and Yuan Zhao (Chengdu University of Information Technology, China)*
10:10-10:25	**A Circuit Defect Detection Method Based on Feature Space Local Anomaly Synthesis and Semi-Supervised Learning Mechanism (#1571347410)** *Zonghang Li, Yundi Liu and Tao Song (China Jiliang University, China); Linfeng Zhou and Mao Xiaoyuan (Shaoxing Test Institute of Quality and Technical Supervision, China); Songxiao Cao, Bin Zhou and ZhiPeng Xu (China Jiliang University, China)*

OVERVIEW OF SESSION VIII

SESSION	SS8 Advanced Computational Algorithms and Multiphysics Modeling for Integrated Systems
VENUE	YAXU Hall (雅叙厅)
TIME	8:30-9:30 November 6th
SESSION CHAIRS	Huan Huan Zhang, Xidian University Qiwei Zhan, Zhejiang University Haoqiang Feng, Zhejiang University
TECHNICAL TALKS	
8:30-8:45	**Multilevel Parallel DGTD Acceleration Using Asynchronous Remote Communication (#1571366496)** *Yunhao Qu (Nanjing University of Science and Technology,China); Qiran Lu (Nanjing University of Science and Technology, China); Hanyu Li and Haijing Zhou (Institute of Applied Physics and Computational Mathematics, China); Mengmeng Li (Nanjing University of Science and Technology & Communication Engineering, China); Dazhi Ding (Nanjing University of Science and Technology, China)*
8:45-9:00	**Electromagnetic Field Analysis of Chip Interconnects Using Enhanced High-Order DGTD Method (#1571354245)** *Zhenzuo Si, Haoqiang Feng and Qiwei Zhan (Zhejiang University, China)*
9:00-9:15	**An Adaptive DG Method for Thermal Analysis of 3D Integrated Systems (#1571351838)** *Haoqiang Feng (Zhejiang University, China)*
9:15-9:30	**AI-Driven Multiphysics Digital Twin and Closed-Loop Optimization for Thermal-Reliability-Aware Design of 3D Chiplet Systems (#1571353939)** *Honghao Jia and Qiwei Zhan (Zhejiang University, China)*

OVERVIEW OF SESSION IX

SESSION	SS9 AI-Assisted TCAD and EDA for Devices and Circuits
VENUE	YAXU Hall (雅叙厅)
TIME	9:40-10:40 November 6th
SESSION CHAIRS	Da-Wei Wang, Hangzhou Dianzi University Shuo Zhang, Zhejiang University Dan Shi, Beijing University of Posts and Telecommunications Yinliang Diao, South China Agricultural University
TECHNICAL TALKS	
9:40-9:55	**Farthest Point Sampling for Carbon Nanotube Deep Potentials (#1571354058)** *Changhong Zhang, Jie Liang, Yi Li, Zhenyu Wang, Lei Zhang, Haoyuan Li and Hanshen Xin (Shanghai University, China)*
9:55-10:10	**Physics-Constrained Neural Modeling of Dissipative Quantum Transport in Two-Dimensional MOSFETs and TFETs (#1571354348)** *Jintang Wang, Qi Shen, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)*
10:10-10:25	**Prediction of Far-Field Antenna Parameters Using Adaptively Sampled Spherical near-Field Data (#1571352039)** *Xiaodong Chen and Yinliang Diao (South China Agricultural University, China)*
10:25-10:40	**AI Modeling and Prediction of Electromagnetic Interference for Metamaterial-Shielded Precision Detection Environments (#1571353922)** *Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Ze Chen (Yancheng Teachers University, China); Kun Zhang (Institute of Mechanics, Chinese Academy of Sciences, China); Dandan Qu (Institute of Mechanics Chinese Academy of Sciences, China); Yang Meng (China Academy of Science, China)*

OVERVIEW OF SESSION X

SESSION	SS10 Power Integrity and EMI Protection for Power Delivery Networks
VENUE	HUANYING Hall (环瀛厅)
TIME	10:50-12:05 November 6th
SESSION CHAIRS	Yusheng Hu, Jimei University Jiazheng Xu, ZTE Corporation
TECHNICAL TALKS	
10:50-11:05	**Power Tree Analysis with Multi-Phase Modeling and Nonlinear Converter Efficiency (#1571364152)** *Qiwen Yan (Southwest University of Science and Technology, China); Yin Sun, Yuteng Zheng, Mingjun Li and Xu Wang (DeTooLIC Technology Co., China); Xiaohe Chen (China University of Petroleum, China); Shufang Li (Beijing University of Posts and Telecommunications, China)*
11:05-11:20	**A Comparative Electrothermal Study of Vertical and Lateral Power Delivery in a Multilayer PCB (#1571364170)** *Hangkai Zhang (Zhejiang University, China); Xu Wang (DeTooLIC Technology Co., China); Xinglin Sun (Zhejiang University, China); Jun Fan (Missouri University of Science and Technology, USA)*
11:20-11:35	**Stopband Analysis of a Stepped-Impedance EMI Power Filter Using a Cascaded Network Model (#1571354367)** *Chenghao Lan, Yusheng Hu, Yudong Zhang and Yaoquan Ou (Jimei University, China)*
11:35-11:50	**Mechanism and Protection of DC TOV (#1571360172)** *Jia zheng Xu (ZTE Corporation, China)*
11:50-12:05	**Automated Modeling for On-Silicon PDNs: From GDS to Impedance (#1571370239)** *Jiahong Chen and Si-Ping Gao (Nanjing University of Aeronautics and Astronautics, China); En-Xiao Liu (Institute of High Performance Computing, Singapore); Wenjian Yu (Tsinghua University, China)*

OVERVIEW OF SESSION XI

SESSION	SS11 Physics-Based Modeling and Design Optimization of Interconnects and Wireless Systems
VENUE	HUIYUAN Hall (慧源厅)
TIME	10:50-12:05 November 6th
SESSION CHAIRS	Ping Li, University of Electronic Science and Technology of China Xiaochun Li, Shanghai Jiao Tong University Min Tang, Shanghai Jiao Tong University Yuxian Zhang, Anhui University Wei Wang, Hangzhou Dianzi University
TECHNICAL TALKS	
10:50-11:05	**RDL Interconnect Response Prediction via Parameterized Local-Model Reuse and Assembly (#1571363734)** *Yan Wang and Anqi Wang (Anhui University, China)*
11:05-11:20	**Physics-Based Inverse Methods for Impedance Corners and Material Extraction (#1571364597)** *Qihang Shang (DeTooLIC Ltd. Technology, China); Tianqi Zhou (Ningbo University, China); Wenzhi Wang (DeTooLIC Ltd. Technology, China)*
11:20-11:35	**Space Mapping Assisted Design Centering of High-Speed Connectors (#1571367205)** *Chaoqiang Zang (HUNAN University, China); Yuping Dan (xFusion Digital Technologies Ltd., China); Chi Lidong (Hunan University, China); Lei Deng (LinkE Technologies, China); Yinzhu Tang (Southwest University of Science and Technology, China); Yihong Qi (unknown)*
11:35-11:50	**A Dual-End Compact UWB Circularly Polarized Ring Patch Antennas (#1571353726)** *Wenzhe Gu, Xiong Yang and Yiyuan Luo (Huizhou University, China); Shiming Qin (Xi'an Aeronautical Computing Technology Research Institute, China)*
11:50-12:05	**High-Purity Broadband OAM Vortex Beam Generation Through 3D-Printed Transmit Array in Terahertz Communication Systems (#1571354775)** *Muhammad Ishfaq (Lanzhou University of Technology, China); Hajra Khan (Comsats University Islamabad Abbottabad Campus, Pakistan); Samir Salem Al-Bawri (Universiti Kebangsaan Malaysia (UKM), Malaysia); Syed Muzahir Abbas (Macquarie University, Australia)*

OVERVIEW OF SESSION XII

SESSION	SS12 Advanced Multiphysics Analysis and Coupled-Physics Mechanisms
VENUE	YAXU Hall (雅叙厅)
TIME	10:50-11:50 November 6th
SESSION CHAIRS	Hua Guang Bao, Nanjing University of Science and Technology Yue Zhang, East China University of Science and Technology Tiancheng Zhang, Nanjing University of Science and Technology
TECHNICAL TALKS	
10:50-11:05	**A Finite-Difference-Based Fluid-Thermal Coupling Framework with SOR-Accelerated PISO for Microchannel Cooling in Power Amplifiers (#1571347088)** *Rengjun Zhou, Yan Peng, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)*
11:05-11:20	**An Accurate Electromagnetic-Fluid Multiphysics Model for High-Power Plasma Limiters (#1571348053)** *Dongming Liu, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China); Haoran Qin (Jiangsu University Of Science And Technology, China)*
11:20-11:35	**Three-Dimensional FDTD Method of Bidirectional Magneto-Mechanical Coupling in Magnetostrictive Layers of Magnetoelectric Antennas (#1571366499)** *Zheng Zhang, Lixia Yang and Yingsong Li (Anhui University, China); Chengjie Zuo (University of Science and Technology of China, China); Shitao Chen (Anhui University, China)*
11:35-11:50	**Intelligent Topology Optimization of Microstrip Ring Filters via Constrained Sampling Strategy (#1571347863)** *Chong Huang, Wen Fan, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)*

OVERVIEW OF YOUNG PROFESSIONALS FORUM

VENUE	**Venue: Qier Hall, Haining Yuanzheng Hotel** **Round-trip shuttle service will be provided. The shuttle will depart from the Hangzhou Blossom Water Museum Hotel at approximately 12:30 PM on November 5, after lunch, and return to Hangzhou after the session for the conference banquet that evening.** **地点：海宁圆正酒店启尔厅** **会议提供往返大巴接送。大巴将于 11 月 5 日午餐后约 12:30 从杭州宝盛水博园大酒店出发，活动结束后返回杭州，参加当晚的大会晚宴。**
TIME	15:30-17:00 November 5th
SESSION CHAIRS	Syed Muzahir Abbas, Macquarie University, Australia
INTRODUCTION	**Young Professionals Forum – Career Development and Growth Pathways** This session focuses on the professional development of young engineers, aiming to create an open and collaborative platform for sharing experiences and fostering mutual growth among early-career professionals. The discussion will revolve around three key topics: **1. Establishing a Clear Career Vision** – How can young professionals define their long-term career direction and develop a practical roadmap for continuous growth in the early stages of their career? **2. Developing Core Technical and Soft Skills** – What are the essential competencies that will shape the future of the electromagnetic and high-speed industries, and how can young engineers effectively enhance these skills to stay competitive? **3. Building and Sustaining Professional Networks** – How can young professionals actively cultivate high-quality connections and leverage professional communities to accelerate their career advancement? Through sharing experiences, challenges, and success stories, this session encourages participants to explore actionable strategies for achieving sustainable professional development in the dynamic field of electromagnetics.

OVERVIEW OF IBIS SUMMIT CHINA

VENUE	YUQING Hall (玉清厅)
TIME	8:30-11:50 November 6th
SESSION CHAIRS	Kinger Cai, Arm Limited, USA Ling Zhang, Zhejiang University, China
INTRODUCTION	The IBIS Summit is an international technical forum organized by the IBIS Open Forum, bringing together experts and engineers in high-speed system design, signal integrity, and modeling to discuss the latest standards and technology trends. IBIS Summit China is one of its key regional events, attracting leading companies and research institutes across China every year. In 2026, the IBIS Summit China will be concurrently held with the 2026 International Workshop on Advanced Interconnects (WAI 2026) in Hangzhou, China. This strategic partnership is aimed to synergize the two communities, with a focused exploration of cutting-edge topics on high-speed interconnects, SI/PI, and chip-package EMC. The joint event is expected to bridge the gap between standardization, academic research, and industrial application, accelerating innovations for the future of AI.
INVITED TALKS	**AI-Assisted Signal Integrity Analysis and Optimization for High-Speed Links** *Da-Wei Wang, Professor at Hangzhou Dianzi University, China* **Efficient PDN Optimization Method Based on Equivalent Circuit Fine-Tuning** *Li Jiang, PhD Student at Zhejiang University, China* **A Phase-Noise-Based Method for Calculating Random Jitter Amplification in Clock Channels** *Tao Wei, PhD Student at Xidian University, China* **Theory and Techniques of RF Probe Calibration: From Parasitic Extraction of Calibration Standards to Calibration Algorithm** *Jiefeng Zhou, Nanjing University of Aeronautics and Astronautics, China* **ML for Practical PCB PDN Design** *Chulsoon Hwang, Associate Professor at Missouri University of Science and Technology, USA* **Multi-Objective Inverse Optimization of High-Speed Interconnects Using Cascaded Deep Neural Network** *Yicheng Zhang, PhD Student at Zhejiang University, China*

TITLE	**AI-Assisted Signal Integrity Analysis and Optimization for High-Speed Links**
TIME	08:30 – 09:00, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Da-Wei Wang, Professor at Hangzhou Dianzi University, China

ABSTRACT

The growing complexity of high-speed interconnects in advanced packaging and 3D heterogeneous integration motivates AI-assisted approaches to improve the efficiency of signal integrity modeling, analysis, and optimization. This talk will present our recent research efforts in AI-assisted SI analysis and optimization for high-speed interconnects, covering surrogate modeling, efficient simulation, and intelligent optimization techniques. Representative applications will be discussed to demonstrate how data-driven methods can be integrated with physics-based approaches to improve the accuracy and efficiency of SI analysis and design.

Furthermore, considering the increasing interactions among electromagnetic, thermal, and power-related effects in advanced integrated systems, recent progress in multiphysics interconnect modeling, integrity analysis, and co-optimization will also be introduced. Finally, remaining challenges and future research directions toward AI-assisted design of high-performance integrated systems will be discussed.

TITLE	**Efficient PDN Optimization Method Based on Equivalent Circuit Fine-Tuning**
TIME	09:00 – 09:30, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Li Jiang, PhD Student at Zhejiang University, China

ABSTRACT
This work presents an efficient PDN optimization method based on equivalent circuit fine-tuning. A generalized inductance formulation is first derived for arbitrary pattern containing several power and ground vias. The exact current coefficients of different vias are then determined through rigorous theoretical derivation. An equivalent circuit model of PDN with a special property is then constructed or transformed from PDN S-parameters. When PDN structural modifications occur, the equivalent circuit is efficiently fine-tuned using the inductance variations obtained from the proposed inductance formulation. Case studies, including experimental measurements, corroborate the practicality and effectiveness of the proposed approach.

TITLE	**A Phase-Noise-Based Method for Calculating Random Jitter Amplification in Clock Channels**
TIME	9:30 – 10:00, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Tao Wei, PhD Student at Xidian University, China

ABSTRACT
As clock frequencies and data rates continue to increase, random jitter and its amplification through frequency-dependent interconnects have become important challenges in high-speed system design. This speech presents a phase-noise-based approach for analyzing and calculating random jitter amplification in clock channels. By incorporating the higher-order harmonics of realistic clock waveforms, the method provides a more accurate description of jitter propagation. The underlying mechanism of jitter amplification will be discussed in terms of the relative attenuation of jitter sidebands and clock harmonics. Simulation and measurement results from transmission lines and DDR5 channels will be presented to demonstrate the approach and illustrate how channel response, clock frequency, and jitter bandwidth influence jitter amplification. These findings offer practical insight for jitter budgeting, channel optimization, and timing-margin management in high-speed systems.

TITLE	**Theory and Techniques of RF Probe Calibration: From Parasitic Extraction of Calibration Standards to Calibration Algorithm**
TIME	10:00 – 10:30, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Jiefeng Zhou, Nanjing University of Aeronautics and Astronautics, China

ABSTRACT
Broadband on-wafer S-parameter measurement is essential for signal-integrity analysis of high-speed AI-chip channels, yet its accuracy is severely limited by RF probe parasitics, crosstalk, nonideal calibration standards, and complex error terms. This report presents a systematic calibration theory and technique for broadband on-wafer S-parameter measurement. It covers optimization-based parasitic extraction of calibration standards, a symmetric differential probe calibration method, and a 64-term error model for differential probe calibration up to 110 GHz. The proposed methods provide effective support for signal-integrity testing of high-speed AI-chip channels.

BIOGRAPHY
Jiefeng Zhou (Member, IEEE) received the B. S. degree in electronic information engineering from Xidian University, Xi'an, China, in 2020, and the Ph. D degree in electronic information from Zhejiang University, Hangzhou, China, in 2025. He is currently an associate researcher at Nanjing University of Aeronautics and Astronautics.

His current research interests include signal integrity (SI), on-wafer S-parameter measurement, Spoof Surface Plasmon Polaritons (SSPPs), and metasurfaces. He was the recipient of the Honourable Mention Paper Award in 2022 Asia-Pacific International Symposium on Electromagnetic Compatibility and the Best Student Paper Award in 2023 and 2025 International Conference on Microwave and Millimeter Wave Technology.

TITLE	**ML for Practical PCB PDN Design**
TIME	10:50 – 11:20, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Chulsoon Hwang, Associate Professor at Missouri University of Science and Technology, USA

ABSTRACT
With the growing complexity of modern hardware systems and increasingly short design cycles, there is a compelling need for faster, more efficient PDN design methodologies. Machine learning can play a pivotal role by enabling capabilities not possible with conventional approaches. This talk will introduce recent progress in machine-learning applications for PDN design, with a focus on practical PCB-level PDN design synthesis.

TITLE	**Multi-Objective Inverse Optimization of High-Speed Interconnects Using Cascaded Deep Neural Network**
TIME	11:20 – 11:50, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Yicheng Zhang, PhD Student at Zhejiang University, China

ABSTRACT
This talk presents a novel multi-objective inverse optimization method for high-speed interconnects based on a cascaded deep neural network (DNN) structure, enabling efficient simultaneous optimization of characteristic impedance, insertion loss, and far-end crosstalk (FEXT). Parameter optimization for high-speed interconnects is essential to ensuring signal integrity and electrical performance in complex designs such as multilayer printed circuit boards (PCBs) and chiplets. Conventional optimization approaches often require numerous iterations, making them highly time-consuming, especially in high-dimensional parameter spaces. In this talk, we introduce a DNN-based method that cascades an inverse-prediction network with a forward-prediction network to achieve multi-objective optimization by adjusting trace width, trace spacing, and pair-to-pair distance. Furthermore, we demonstrate how integrating integer programming enables the optimization of multilayer PCB stack-ups and the design parameters of individual signal layers within seconds, significantly improving efficiency compared with conventional optimization approaches.

POSTER SESSIONS

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
1	1571347054	A Preconditioned Domain Decomposition Framework for Multiphysics Analysis of RF Devices	*Huan Wang, Wenwei Zhang, Wenchi Huang, Jianing Cao, Jiaqi Kang, Chenche Zhao, Mingyao Xia*	*Peking University, China*
2	1571347908	Broadband EMI Suppression Mechanism of an Asymmetric Hybrid Inductor	*JinLiang Wang, Jinling Zhang, ShuangQing Xiong*	*Beijing University of Posts and Telecommunications, China*
3	1571351036	Efficient Broadband Modeling of High-Speed Fixtures Using an Enhanced Stub Model	*Tao Zhou, Xu Wang, Bo Pu, Yanwu Wang, Jun Fan*	*Southwest University of Science and Technology, China; DeTooLIC Ltd. Technology, China; Missouri University of Science and Technology, USA*
4	1571352562	Double-Layer Triple-Band Circularly Polarized Reflectarray Antenna Producing Five Beams	*Lingfeng Xu*	*Nanjing University of Science and Technology, China*
5	1571353588	Graph Neural Network Surrogates for Coupled Electrothermal Analysis of 3D Power Delivery Networks	*Jamila Rzali*	*Zhejiang University, China*
6	1571354009	Machine-Learning-Assisted Wafer-Scale Prediction of IGZO Thin-Film Thickness Distributions Using a DeepONet Surrogate Model	*Junwei Wang, Chenyang Sun, Zhiyu Ma, Yi Li, Jie Liang*	*Shanghai University, China*
7	1571354070	Hybrid Bayesian Work Function Design for Symmetric RFETs	*Chenyang Sun, Junwei Wang, Zhiyu Ma, Jie Liang, Yi Li*	*Shanghai University, China*
8	1571354103	Reducing Low-Frequency CM Noise in Power Converters by Digital Active Closed-Loop Control	*Wenqi Lin, Qidong Bao, Xinglin Sun*	*Zhejiang University, China*
9	1571354231	Process-Sequential Modeling of TCB and Underfill Curing for 2.5-D Micro-Bump Interconnects with AI-Assisted Parameter Exploration	*Jiachen Yang*	*Hangzhou Dianzi University, China*
10	1571355571	Using a Spatial Null to Test Scalar Electric-Field Probe Interpretation	*Zipeng Chen, Wenxiao Fang, Huachun Wang*	*Sun Yat-sen University, China*
11	1571358782	Reusable GNNs for S-Parameter Extraction and SI Optimization of Coupled PCB Interconnects	*Junjie Peng, Ping Li*	*University of Electronic Science and Technology of China, China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
12	1571359628	Feasibility-First Two-Stage Optimization for Target-Impedance-Constrained PDN Decap Design	*Qiyu Jiang, Shufang Li, Xiaohe Chen*	*Beijing University of Posts and Telecommunications, China; China University of Petroleum (Beijing), China*
13	1571359650	Noise Coupling in Multilayer PCBs: Mechanism Analysis and Simulation-Measurement Correlation	*Cailiang Fu, Anfeng Huang, Yin Sun*	*Southwest University of Science and Technology, China; DeTooLIC Technology Co., China*
14	1571359868	Mapping Multiple Noise-Source Contributions from Synchronous near-Field Scans	*Hailing Zhao*	*Southwest University of Science and Technology, China & Mianyang, China*
15	1571360218	Impact of Frequency-Dependent High-Voltage Port Impedances on Vehicle-Level Radiated-Emission Prediction for Electric Vehicles	*Leixin Li, Li Zhai, Haonan Xu*	*Beijing Institute of Technology, China*
16	1571360270	Experimental Study of the Effect of High- and Low-Voltage Crosstalk on Common-Mode Interference Current in an Automotive FlexRay Bus	*Haonan Xu, Li Zhai, Leixin Li*	*Beijing Institute of Technology, China*
17	1571363991	Residual Neural Network for Tabbed-Routing Impedance Prediction in via Pin Fields	*Ren Qingyuan, Jie Li, Qihang Shang*	*City University of Hong Kong, Hong Kong; Southwest University of Science and Technology, China; DeTooLIC Ltd. Technology, China*
18	1571364740	Impedance Correction for PCB de-Embedding at 50 GHz and Above	*Anfeng Huang, Cailiang Fu*	*DeTooLIC Technology Co., China; Southwest University of Science and Technology, China*
19	1571365103	PDN Power-Plane Shape Optimization Through Vertex-Based Expansion for DC Impedance Reduction	*Chenxu Zhang, Ling Zhang, Er-Ping Li*	*Zhejiang University, China*
20	1571366768	Thickness-Constrained Design of Silicone-Bonded Nanocrystalline Sheets with Prescribed Magnetic Response	*Qiusen He, Bing Sun, Xiaoping Li, Xinglin Sun*	*Zhejiang University, China; Tianjin University, China; Swust University, China*
21	1571367232	FDTD Solution of the Landau-Lifshitz-Gilbert Equation for Ferromagnetic Resonance Simulation	*Zhidan Qiu, Shitao Chen, Lixia Yang, Yingsong Li, Chengjie Zuo*	*Anhui University, China; University of Science and Technology of China, China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
22	1571367415	Extraction of Parameters for the GaN Physics-Based Compact Model Based on Multi-Constraint Fitting	*Junhao Shen*	*Nanjing University of Science and Technology, China*
23	1571367694	Wideband Duplexer for EMC-Related Test Applications	*Wen Tao, Xiong Chen*	*Xi'an Jiaotong University, China; Xian Jiaotong University, China*
24	1571368429	Band-Specific Matching Networks for Broadband High-Power Amplifiers	*Zhengmin Chen, Xiong Chen*	*Xi'an Jiaotong University, China; Xian Jiaotong University, China*
25	1571369558	Thermal Dissipation of GaN Power Chip Package With Heat Slug on Die	*Shuaifei Wang, Jicun Lu, Miaosen Yang, Ruishuang Yuan*	*Shanghai DianJi University, China*
26	1571369748	Pulsed Magnetic Field Immunity of Six-Axis Force Sensors	*Xin Cheng, Ying-Hua Zhang, Xinxin Tian, Weiheng Shao, Mingbin Hu, Shao E*	*Guangdong University of Technology, China; Maritime Safety Administration, China; CEPREI Laboratory, China; China Electronic Product Reliability and Environmental Testing Research Institut, China; China Electronic Product Reliability and Environmental Testing Reasearch Institute, China*
27	1571369856	Solder Joint Quality and Reliability of Perforated Cu Clip in Power Module Package	*Penglin Zhang, Jicun Lu, Miaosen Yang, Ruishuang Yuan*	*Shanghai DianJi University, China*
28	1571369902	Event-Resolved Conducted EMI of Top-Side Interconnects in a Si/SiC Hybrid Switch	*Xinzheng Hu, Shaotong Yang, Yan Li*	*China Jiliang University, China*
29	1571369962	Equal-Area Pattern Redistribution in a Three-Layer Broadband Microwave Absorber	*Hualei Zhu, Longping Chen, Yan Li*	*China Jiliang University, China*
30	1571370822	Efficient Markov Simulation of Error Bursts in Coded Wireline Links	*Yuhao Huang, Hanrui Huyan, Xiuqin Chu*	*Xidian University, China; Xi'an University of Electronic Science and Technology, China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
31	1571370915	Hierarchical Volterra Modeling for Nonlinear High-Speed I/O Circuits Using DC/AC Characterization	*Yajun Lv*	*Xidian University, China*
32	1571370947	Thermal Optimization of Si MOSFET Power Package on Solid-State Circuit Breaker PCB Board	*Tao Zhou, Bowen Yang*	*Shanghai DianJi University, China*
33	1571370953	CER-Aware FEC Redundancy Optimization for PAM4 Chiplet Links With DFE-Induced Error Propagation	*Yuhao Huang, Shen Chun, Xiuqin Chu*	*Xidian University, China; Xi'an University of Electronic Science and Technology, China*
34	1571371028	UV-Assisted Thermal Debonding of a Dynamic Alkoxyamine Wafer Temporary Adhesive	*Rui Li, Jicun Lu*	*Shanghai DianJi University, China*
35	1571371069	Effects of Conventional Annealing on the Magnetic Properties and Giant Magnetoimpedance of Co-Based Magnetic Microwires	*Shihong Mo, Jicun Lu*	*Shanghai DianJi University, China*
36	1571371078	Design and Characterization of Coplanar Nested-Coil FPC Transformers	*Tian Yang, Weisi He*	*Shanghai DianJi University, China*

DIRECTIONS TO HANGZHOU BLOSSOM WATER MUSEUM HOTEL

Driving by Yourself



Please search for "Hangzhou Blossom Water Museum Hotel" in GPS. The navigation system will automatically plan the optimal route according to your current location.

Parking: The hotel provides 600 underground parking spaces.

By Taxi



Take a taxi and set your destination to: Hangzhou Blossom Water Museum Hotel.

By Metro



From Hangzhou Xiaoshan International Airport:
→ Enter Xiaoshan International Airport Station.
→ Take Metro Line 7.
→ Transfer according to the latest metro guidance toward Genwen Road Station.
→ Exit at Genwen Road Station (Exit A1).
→ Walk approximately 2.2 km to reach the hotel.

From Hangzhou East Railway Station:
→ Enter Hangzhou East Railway Station Metro Station.
→ Take the metro toward Genwen Road Station.
→ Exit at Genwen Road Station (Exit A1).
→ Walk approximately 2.2 km to reach the hotel.

ACCOMMODATION

Special rates have been negotiated for the WAI 2026 attendees at Hangzhou Blossom Water Museum Hotel. If you need to book a room, please contact the hotel before November 1, 2026, quoting the name of the conference to make a reservation at the special rate.

Hotel Name：

Hangzhou Blossom Water Museum Hotel
杭州宝盛水博园大酒店
Hotel Address：
No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China
杭州市萧山区水博路 118 号
Hotel Phone Number：
+86-571-83500888



Recommendations for other hotels:

Hotel Name：

Hangzhou Shuiboyuan Daogu Hotel
杭州水博园 • 道谷酒店
Hotel Address：
No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China
浙江省杭州市萧山区水博路 118 号
Hotel Phone Number：
+86-571-86009099



Hotel Name：

Quan Ji Hotel (Hangzhou Xiaoshan Jiangnan Science City)
全季酒店(杭州萧山江南科技城店)

Hotel Address：

No.708 Changxiang Road, Xiaoshan District, Hangzhou, Zhejiang, China
浙江省杭州市萧山区畅想路 708 号

Hotel Phone Number：

+86-571-28899888



Hotel Name：

Orange Hotel (Hangzhou Xiaoshan Jiangnan Science City)
橘子酒店（杭州萧山江南科技城店）

Hotel Address：

23 Qianwanzhigu, Guming Road, Xiaoshan District, Hangzhou, Zhejiang, China
浙江省杭州市萧山区鼓鸣路钱湾智谷 23 幢

Hotel Phone Number：

+86-571-82961818



ABOUT HANGZHOU

Historical Significance




Hangzhou is a big city steeped in a rich, millennium-long history and is celebrated as one of China's seven ancient capitals. Central to its cultural legacy is the West Lake, a UNESCO World Heritage Site that has inspired poets, scholars, and artists for centuries and stands as a timeless symbol of Chinese aesthetic harmony. The city's heritage is further underscored by the Grand Canal, the world's longest man-made waterway, highlighting Hangzhou's enduring role as a vital nexus of historical commerce and vibrant cultural exchange.

Strategic Location



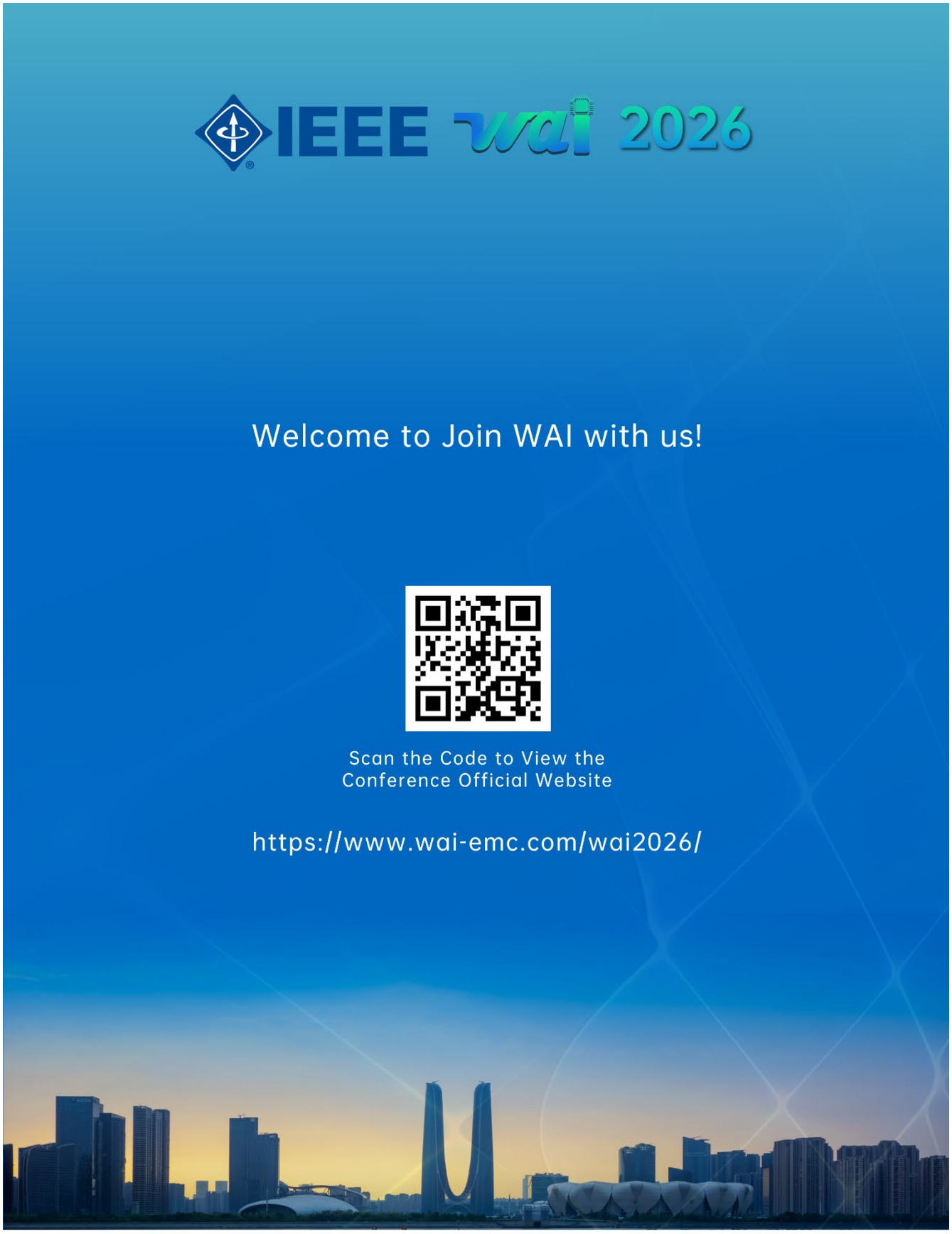

Situated on the southeastern coast of China, Hangzhou serves as the political, economic, and cultural center of Zhejiang Province. Nestled at the southern core of the Yangtze River Delta—one of the world's most economically dynamic regions—the city boasts a highly advantageous geographic position. It is seamlessly connected to Shanghai to the northeast and Ningbo to the east, making it a pivotal transportation and logistics hub that effectively bridges domestic networks with global markets.

Economic Development & Innovation





Hangzhou is globally recognized as a premier hub for the digital economy, technological innovation, and modern entrepreneurship. Often referred to as China's "Silicon Valley," it is home to world-renowned technology enterprises such as Alibaba and a thriving ecosystem of high-tech startups and research institutions. Supported by a robust advanced manufacturing sector, comprehensive e-commerce infrastructure, and a strong commitment to green and sustainable development, Hangzhou continues to be a leading driver of China's modern economic growth and innovation.


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