WAI 2026 Hangzhou, China November 4 – 6, 2026

2026 International Workshop on
Advanced Interconnects
Hangzhou, China

WAI 2026

November 4 – 6, 2026

Final Program



ZHEJIANG UNIVERSITY

DeToolIC -德图科技-

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DeToolIC
-德图科技-

官网 公众号

企业简介 > COMPANY PROFILE

宁波德图科技有限公司是一家专注于集成电路后端系统EDA仿真设计工具研发的高新技术企业。德图科技以先进封装为突破口，面向芯片、封装、PCB及整机系统等多层级互连场景，致力于构建以信号完整性（SI）、电源完整性（PI）、电磁兼容（EMC）和多物理场仿真为核心的设计、分析与优化平台，打造一站式互连系统EDA解决方案。

芯片 > 封装 > PCB > 系统 | 信号完整性 SI | 电源完整性 PI

核心团队 > CORE TEAM

德图科技创始团队由IEEE Fellow、知名高校专家及国际EDA系统应用专家组成，具备扎实的理论基础、丰富的软件研发经验和工程应用能力。依托自主研发的高精度、高效率仿真算法，德图科技持续推进核心技术创新及国产EDA工具的工程化应用。

> 20%
Ph.D. 博士占比

15+
Self-developed 产品

6
Sites in PRC 全国布局

业务覆盖 > BUSINESS COVERAGE

先进封装 | 传统封装及PCB等

德图可提供大通流多物理场解决方案，以及面向高频高速场景的 SI / PI / EMC "Die-PKG-PCB-System" 全链路解决方案，助力客户缩短研发周期，提升系统性能、稳定性与可靠性。除自主EDA软件产品外，德图科技还提供SI/PI方案设计、仿真分析、测试验证、技术咨询与培训等专业服务，为产品研发与工程落地提供全流程支持。

应用领域 > APPLICATION FIELDS



DeToolIC
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从芯片到系统 高速互连设计仿真

一站式 EDA 工具与工程服务，覆盖 PI / SI / EMC 全流程

PDN系统"电源完整性"及"多物理场"解决方案

芯片级 DC电 SonicPower WireBond建模 VDMOS仿真 电流密度分布图

先进封装级 DC电 SonicPKG Si - Interposer + RDL + TSV 电压分布云图

封装及PCB板级 DC电磁热 SonicMP 压降分布 温度分布 瞬态电热联仿

ACS参数提取 SonicPI 芯片、封装、PCB、多板及电源阻抗 / 信号S参数分析

高速电路"信号完整性"解决方案

TX 高速无源通道 RX

驱动 IC IBIS-AMI — AC Cap — Connector — 接收 IC IBIS-AMI

SonicViaMaster 过孔建模
SonicPCB 传输线建模
SonicLinkScope 信道传输路径分解
SonicS2SPICE S参数转SPICE等效电路

SonicADL Delta L批量自动化测试
SonicDoEPilot 系统级SI优化
SonicLinkSim 时域通道仿真
SonicSMaster S参数后处理分析

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系统设计
- 系统架构设计
- 原理图 / PCB / 封装设计
- 设计、仿真、测试全流程

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- PCB / PKG / 系统全链路
- SI、PI、EMC
- 电、热、力、可靠性

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- 功能 / 性能 / 可靠性测试
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- Delta L 3.0 / 4.0测试

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- SI / PI / EMC 理论
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安费诺 - 全方位数据中心互联技术

主宰AI丛集算力

从铜缆、光通讯到电源传输、光收发器与先进封装架构，我们以全球化规模与深厚工程实力为后盾，提供业界最完整的数据中心高速互连解决方案。

随着AI算力需求由单一节点演进至机架与超大规模集群（Hyperscale Clusters），安费诺持续突破实体层的传输极限。在深度整合机架与机架之间光互连技术的同时，不断拓展机架内部铜互连完整解决方案，实现GPU到交换芯片柜内scale up互连速率从112G，224G，到448G基于铜材的可持续升级。Paladin HD2作为安费诺主力量产的224G连接器产品，广泛的应用于传统背板高速互连，无中板正交高速互连，线缆背板高速互连。Sentry HD作为Paladin HD2下一代高速铜互连产品，为客户带来448G柜内铜互连的全新体验。

安费诺信息通信（ACS）

作为安费诺的分公司，安费诺信息通信(ACS)是为通信、移动、射频、光学和商业电子市场提供互连解决方案的全球领导者。

我们旨在为服务器、存储器、数据中心、移动、射频、网络、工业、商业设备和汽车应用领域设计和制造提供应用广泛的创新连接器和电缆组件。

安费诺信息通信业务广泛，包括研发、制造和销售等方面，业务领域覆盖全球。我们设计和制造各种创新性连接器和电缆组件，应用领域广泛，包括服务器，存储，数据中心，移动，射频，网络，工业，商业设备和汽车。

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LinkE 领翌智连

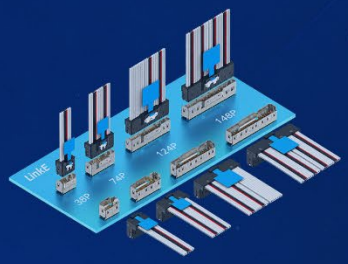
深圳领翌智连科技有限公司是一家专注高频高速互连技术的高科技企业，面向AI算力集群、下一代智算中心、高性能计算应用，致力于高速连接器、高速线缆组件的研发、生产与产业化，并提供系统级信号完整性解决方案。

公司坚持核心技术自主研发，技术团队由院士领衔，拥有60余项海内外自主专利。面向112G、224G以及面向未来的448G高速互连需求，公司持续推进技术创新与产品升级，打造具备国际先进水平的高速互连产品与方案。

PCIe Gen 6/7

连接器线缆组件

（兼容SFF-TA-1016 Footprint）



高速高密度

连接器组件

（支持224G/448G应用）



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HUANERGY

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浙江花园新能源股份有限公司坐落于中国十大名村之一的花园村，由花园集团2017年投资创办，是集研发、生产、销售于一体，专门从事高性能铜箔生产的国家高新技术企业。年产5万吨高性能铜箔项目为浙江省重大产业龙头类项目，填补了浙江省空白。公司致力于高端铜箔的研发和生产，以高端铜箔国产化替代、引领铜箔创新为目标。

花园集团	主营产品	应用领域
中国企业500强	HVLP1-5	高速线路板
中国民营企业500强	RTF1-5	伺服器
中国制造业企业500强	载体铜箔	PCB板
浙商全国500强	埋阻铜箔	5G通讯
浙江省百强企业	高精密压延厚铜箔	汽车电子
	高性能电解厚铜箔	消费电子

研发实力

与浙江大学共建研发平台，设立杭州研究院驱动技术迭代，拥有百余项专利，全系列产品经IATF16949、ISO等权威体系认证。

企业愿景

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以客户为中心，以奋斗者为本，共赢共富共伟大。

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MULTEK 胜宏科技 深南电路

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3673C/D/E/F/G/H/K/L系列 矢量网络分析仪

产品综述

3673系列矢量网络分析仪产品包括3673C(100kHz ~ 14GHz)、3673D(100kHz ~ 20GHz)、3673E(100kHz ~ 26.5GHz)、3673F(100kHz ~ 40GHz)、3673G(100kHz ~ 44GHz)、3673H(100kHz ~ 50GHz)、3673K(10MHz ~ 53GHz)、3673L(10MHz ~ 67GHz)，全系均有二、四两种端口配置可选。3673系列矢量网络分析仪拥有出色的系统动态范围、扫描速度、端口输出功率等指标，该产品可广泛应用于电子、通信、微波等领域，是研发和生产批量测试的常备测试设备。

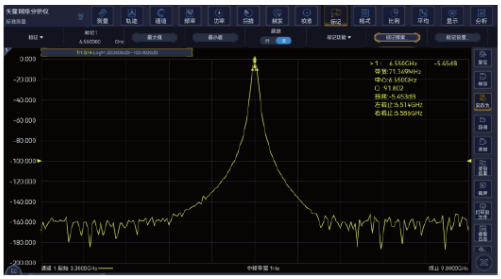


主要特点

- 最优160dB的系统动态范围，助力高性能滤波器等器部件测试
- -60dBm~+20dBm的源功率扫描范围，满足有源器部件测试需求
- 基于DDS架构的激励源技术，更快的扫描速度
- 更全面的频率覆盖，起始频率低至100kHz，具有多种波段机型选择
- 先进的校准技术，丰富的校准类型，支持多通道校准，支持电子校准用户自表征
- 支持Windows及Linux操作系统
- 中/英文操作界面，15.6英寸1920*1080高分辨率多点触控显示屏

160dB系统动态范围，满足更多测试场景

3673系列矢量网络分析仪具有最优160dB的动态范围，可对高抑制比器件进行精确测量，也可以用更大的中频带宽进行器部件测试以获得更快的扫描速度。

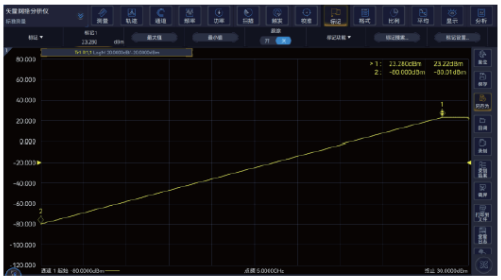


更快的扫描速度

仪器核心激励源采用直接数字频率合成（DDS）技术，相较于上一代产品扫描速度提升4倍。

更宽的功率扫描范围

3673 系列矢量网络分析仪功率扫描范围覆盖 -60dBm~+20dBm（典型值，最优 -80dBm~+23dBm），为有源器部件测试提供更好的支持。同时支持程控步进衰减器选件，进一步扩展至 -120dBm~+20dBm。



规格参数

项目	指标值
频率范围	100kHz~14GHz/20GHz/26.5GHz/40GHz/44GHz/50GHz
	10MHz~53GHz/67GHz
系统动态范围	最优160dB（典型值）
功率扫描范围	-60dBm~+20dBm（典型值、标配）
最大输出功率	高达18dBm，典型值20dBm
扫描点数	最多210001点

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Address:No.98 Xiangjiang Road, Huangdao District, Qingdao, Shandong Province

思仪科技微信公众号
Ceyear Wechat Official Account

姜经理（微信号）
Mr Jiang's Wechat Account

Dloorplf 昆山德普福电子科技有限公司

德普福成立于 2016 年，致力于提供高品质射频通讯零组件及技术服务。创新和品质是公司的核心竞争力。公司的技术团队在微波射频领域拥有相当丰富的设计经验，以及通信测试领域丰富的行业经验。德普福提供完整的射频微波信号连接及行业解决方案，产品涵盖 DC-145GHz 微波电缆组件（SMA、2.92mm、2.4mm、1.85mm、1.0mm、0.8mm、MMPX、GPPO、N 型和 7/16 等，并提供多种铠装护套方案）；多通道射频线缆；精密射频转接器；PCB 板端精密连接器；射频开关模组；射频开关矩阵系统；射频测试探针和自动化测试设备等。



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射频矩阵开关系统





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产品优势

极速求解与超大规模

- FIT 求解核心，支持复杂系统电磁仿真
- GPU 原生加速架构，支持多卡并行计算
- 数十倍求解加速，支持数十亿级网格规模仿真

先进算法与协同仿真

- 自研先进几何共形技术，增强复杂几何适应性
- 同步/异步协同，满足场路联合仿真需求

智能交互与高效流程

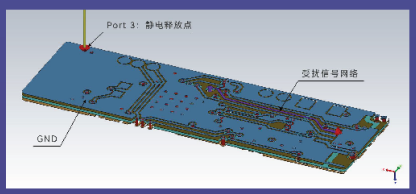
- Python 二次开发，支持流程定制与自动化
- AI 智能体交互，自然语言驱动建模与仿真

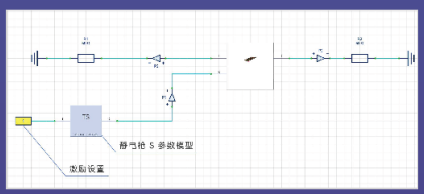
功能特性

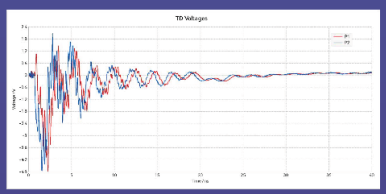
- 建模 - 仿真 - 设计全流程一体化
- EDA 文件导入（.brd / .sip / .mcm / ODB++）
- 3D 文件的导入和导出 （.sat / .sab / .stp / .step）
- 操作与建模历史记录，参数扫描与优化
- FIT 求解器
  - 几何自适应网格线，支持局部网格配置
  - 离散线、面端口，波导端口
  - 色散介质，有耗金属，各向异性材料
  - 先进共形几何增强（ACE）
  - 异步和同步场路协同仿真
- 高性能计算（HPC）
  - 支持 CPU 平台多线程计算
  - 支持单、多 GPU 硬件加速
- 1D/2D/3D 结果处理和可视化

应用实例

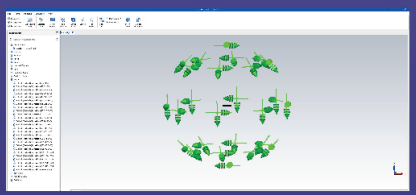
ESD 仿真

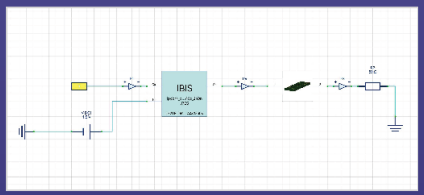


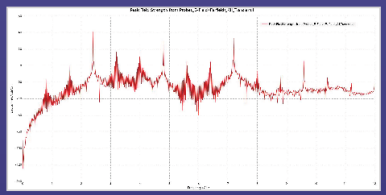




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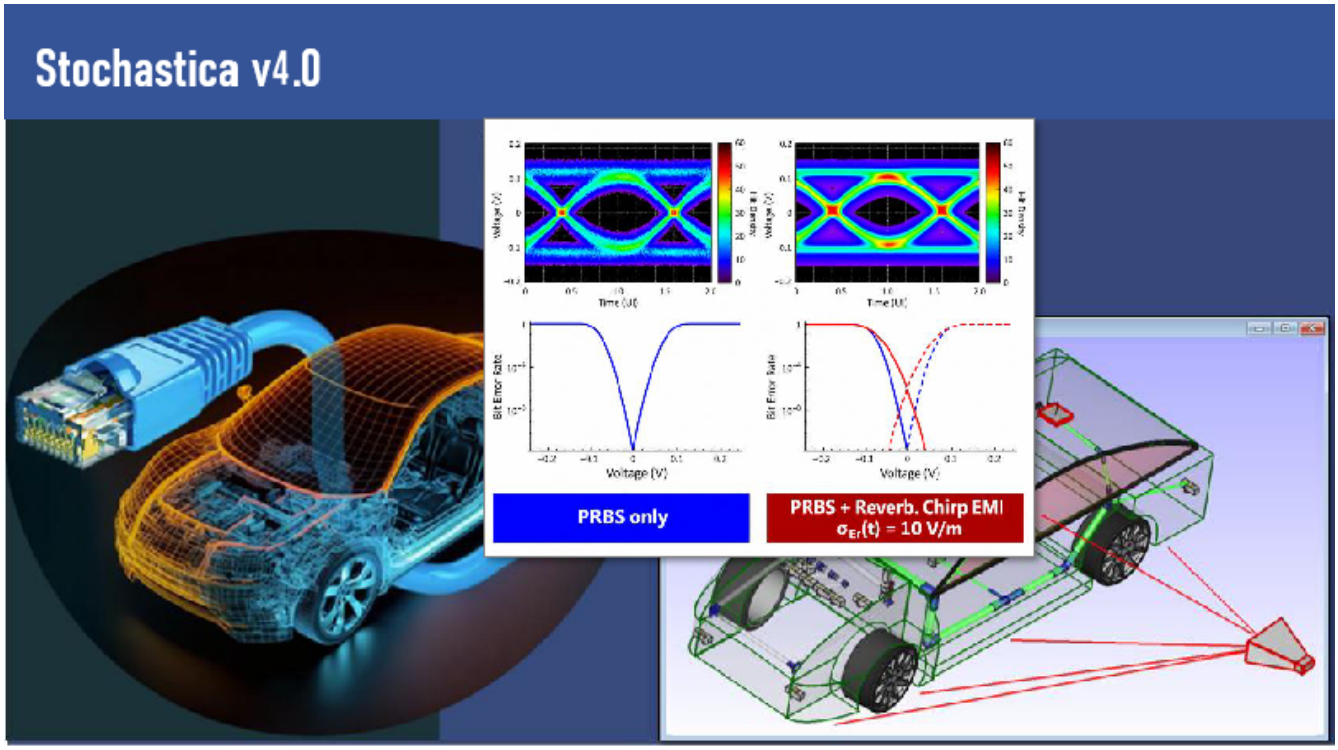
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第叁范式（宁波）科技有限公司成立于 2025 年 12 月，是一家专注于三维全波电磁仿真的工业软件企业，在宁波、上海设有双研发中心。公司核心产品 M3EM Studio 以时域有限积分技术（FIT）求解内核为基础，结合自研的先进共形增强（ACE）技术、多尺度智能网格剖分算法与 GPU 原生加速架构，覆盖从微米级精细结构到米级整机系统的仿真需求，服务于先进封装、消费电子、智能汽车与雷达通信等高端电子研发场景。

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Automotive Ethernet – EMC and SI Co-simulation

RobustPhysics (https://robustphysics.com/) introduces **Stochastica**, a fast, statistics-driven simulation platform for electromagnetic compatibility (EMC) and signal integrity (SI).

Automotive programs need to evaluate worst-case system-level conducted susceptibility (CS) and radiated susceptibility (RS) under complex operational electromagnetic conditions. Fast design-stage simulation is essential for iterative optimization and early mitigation of EMC and SI risks before costly system-level testing. Automotive Ethernet, based on IEEE 802.3, supports data rates up to 10 Gb/s over lightweight, low-cost twisted-pair cables. At 10 Gb/s, the high signaling frequencies and PAM4 modulation make bit-error-rate (BER) margins *design-critical*.

Predicting full system-level EMI for an automotive platform is challenging for several reasons. First, external EMI threats are uncertain and can be defined only statistically. Second, unavoidable variations in the vehicle's internal configuration must be characterized statistically. Third, the vehicle cabin behaves as an electromagnetically complex, semi-reverberant cavity, with strong internal scattering (high Q), significant external-field coupling through *front-door* paths (e.g., antennas) and *back-door* paths (e.g., apertures), and radiation from onboard equipment.

Traditionally, automotive programs use semi-empirical transfer-function models and largely defer definitive risk assessment to *system-level testing* late in the program. Until recently, the main alternative was computational electromagnetic modeling, which can become computationally intensive at higher frequencies and is not inherently statistical.

Enter **Stochastica**—an *ultra-fast, statistics-driven* simulation tool that has been validated experimentally under NASA, DARPA, and Navy SBIR programs. The underlying *statistical wave power flow physics* requires neither numerical meshing nor Monte Carlo iterations, enabling fast, interactive simulation with extensive built-in statistical analysis.

Visit our booth to see **Stochastica** in action.

ROBUSTPHYSICS

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INVITATION FROM THE GENERAL CHAIRS

Dear Colleagues and Friends

On behalf of the 2026 WAI Steering Committee, we are privileged and honored to invite you, your colleagues and families to join us for the third International Workshop on Advanced Interconnects (WAI) from Wednesday, Nov. 4th to Friday, Nov. 6th in Hangzhou, China.

The International Workshop on Advanced Interconnects technically co-sponsored by the IEEE and the IEEE EMC Society is a newly launched event. The scope of this workshop specially addresses the latest development and innovations in the advanced interconnects field. The topics include but are not limited to: advanced interconnects and packaging, signal and power integrity, electromagnetic interference and compatibility (EMI/EMC), electrostatic discharge (ESD) and reliability, multiphysics integrity, modeling, simulation, and design methodologies, AI and intelligent EDA technologies, measurement, testing, and validation, as well as RF, microwave, antennas, and emerging applications and systems.

The IEEE EMC Society is the primary co-sponsor of this event, in collaboration with DetoolTech Ltd, Zhejiang University, Nanjing University of Aeronautics and Astronautics and China University of Petroleum.

We warmly welcome you to join us in Hangzhou in November of 2026 for an outstanding scientific/technical event and an unforgettable experience for you and your family.

WAI 2026 General Chairs



Er-Ping Li, IEEE Fellow

Qiushi Chair Professor, Zhejiang University



Jun Fan, IEEE Fellow

Qiushi Professor, Zhejiang University

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Chair of the Technical Program Committee



Ling Zhang

Zhejiang University

Co-Chairs of the Technical Program Committee



Hanzhi Ma

Zhejiang University



Bo Pu

DetoolTech Ltd



Xiaoning Ye

VP Technical Services, EMC Society

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China



TECHNICAL PROGRAM COMMITTEES

The TPC is led by the TPC Chairs and Co-Chairs including **Prof. Ling Zhang, Prof. Hanzhi Ma, Dr. Bo Pu** and **Dr. Xiaoning Ye**. The Technical Committee members for the 2026 WAI are listed as below (sorted by last name).

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Nanjing University of Aeronautics and Astronautics, China

GENERAL INFORMATION

REGISTRATION

Registration link: https://wai-emc.com/wai2026/registration

Please register an account if new to the Registration site.

Each participant must pay a non-refundable registration fee. **Only registered and paid submissions before 26 October, 2026 will be scheduled in the symposium program.** Inclusion of a submission whether it is an abstract or a full paper in the final Technical Program is guaranteed only after the registration of one of the authors is completed and paid before 26 October, 2026, through the Registration link. **One paid registration can cover a maximum of two submissions.** The abstracts and full papers listed in the final Technical Program will be archived in the WAI 2026 Proceedings after they are presented in the conference, any absent submission will be removed. Further, the full papers archived in the WAI 2026 Proceedings will be further uploaded and archived in the IEEE Xplore (EI indexed).

On-site registration will be available through the Registration Desk during the workshop.

The same fee structure is used for both online and onsite registrations. Registration includes daily tea break, lunches and dinners from November 4 to November 5.

Registration Type	Registration Fee
Student Registration	USD 208 / RMB 1480
Regular Registration	USD 348 / RMB 2480

CONFERENCE VENUE

Hangzhou Blossom Water Museum Hotel (杭州宝盛水博园大酒店)

Hangzhou Blossom Water Museum Hotel is located on the banks of the world-renowned Qiantang River, within the China Water Museum Park in Hangzhou. The hotel is approximately 30 minutes from West Lake and only a short drive from Hangzhou Xiaoshan International Airport.

Surrounded by lush greenery, tranquil lakes, and the magnificent Qiantang River, the hotel provides a unique combination of river views, lake views, and garden landscapes. Covering an area of approximately 112 acres, the hotel has been carefully designed as a distinctive resort-style destination integrating natural scenery, comfortable accommodation, and conference facilities.

Its peaceful environment and convenient transportation make it an ideal venue for WAI 2026 participants.

杭州宝盛水博园大酒店坐落于举世闻名的钱塘江畔，中国水立博物馆园内。酒店距离西湖约 30 分钟车程，距杭州萧山国际机场也仅一小段车程。

酒店四周绿树环绕，静谧的湖泊与壮丽的钱塘江相映成趣，将江景、湖景与园林风光完美融合。酒店占地约 112 英亩，经过精心设计，打造成了一个集自然风光、舒适住宿和会议设施于一体的特色度假胜地。

这里环境宁静，交通也十分便利，是 WAI 2026 参会者的理想下榻之所。







LOCATION MAP AROUND THE CONFERENCE VENUE



★Hangzhou Blossom Water Museum Hotel

Address: No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China

(+86-571-83500888)

Website: https://www.hangzhoublossomwater.cn/

REGISTRATION DESK

Admission to all sessions and hosted functions requires the attendance identification. Please wear your name badge at all times.

Badge and other workshop materials can be picked up from the Registration Desk during the workshop for the participants registered online. On-site registration will also be available through the Registration Desk.

Registration Desk time

☐ November 3, Tuesday	14:00 - 19:00
☐ November 4, Wednesday	7:30 – 17:00
☐ November 5, Thursday	7:30 – 17:00
☐ November 6, Friday	7:30 – 9:00

Registration Desk will be located in the front lobby of the conference venue.

Hangzhou Blossom Water Museum Hotel

杭州宝盛水博园大酒店

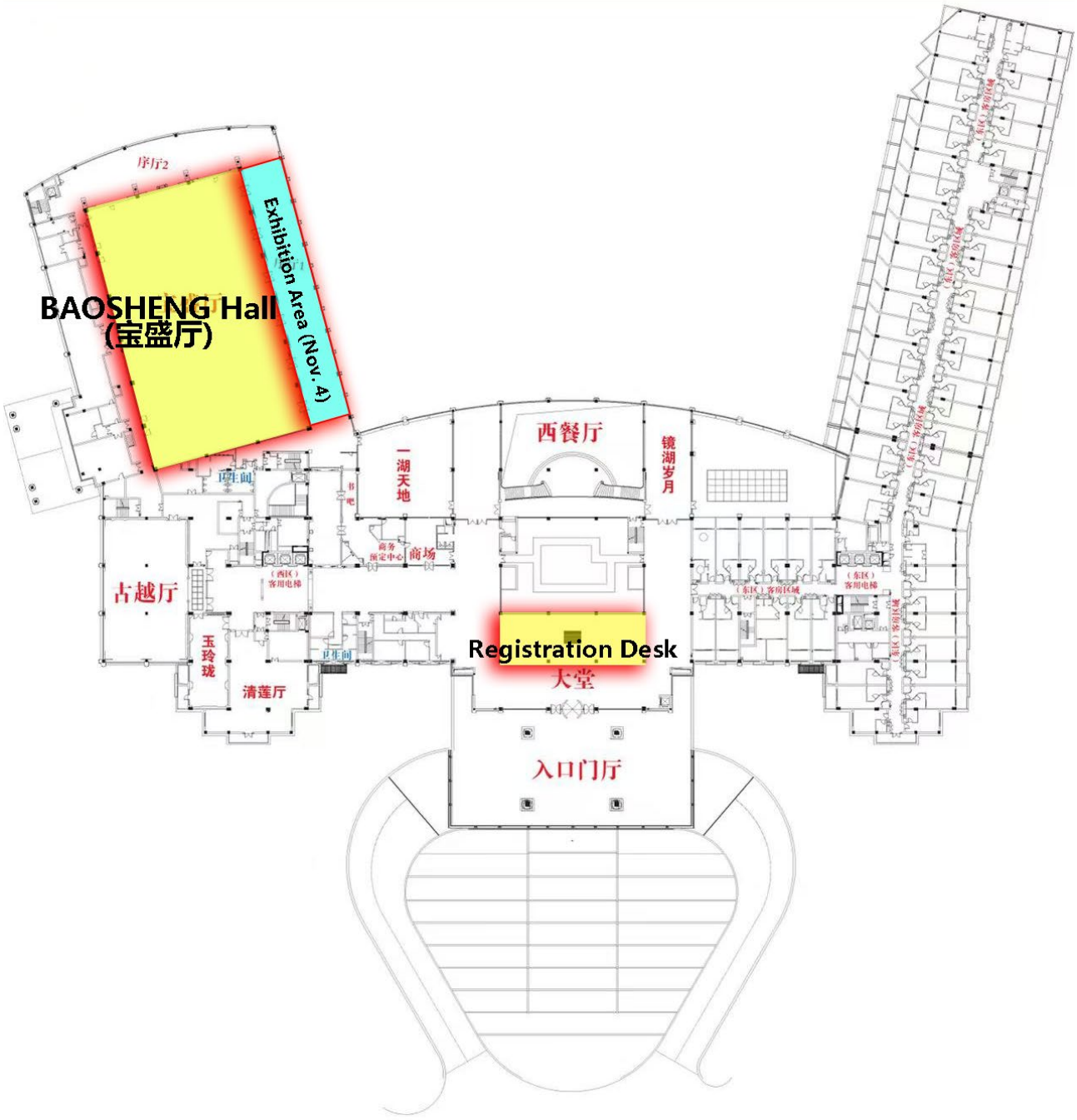
No.118 Shuibo Road, Xiaoshan District, Hangzhou, Zhejiang, China



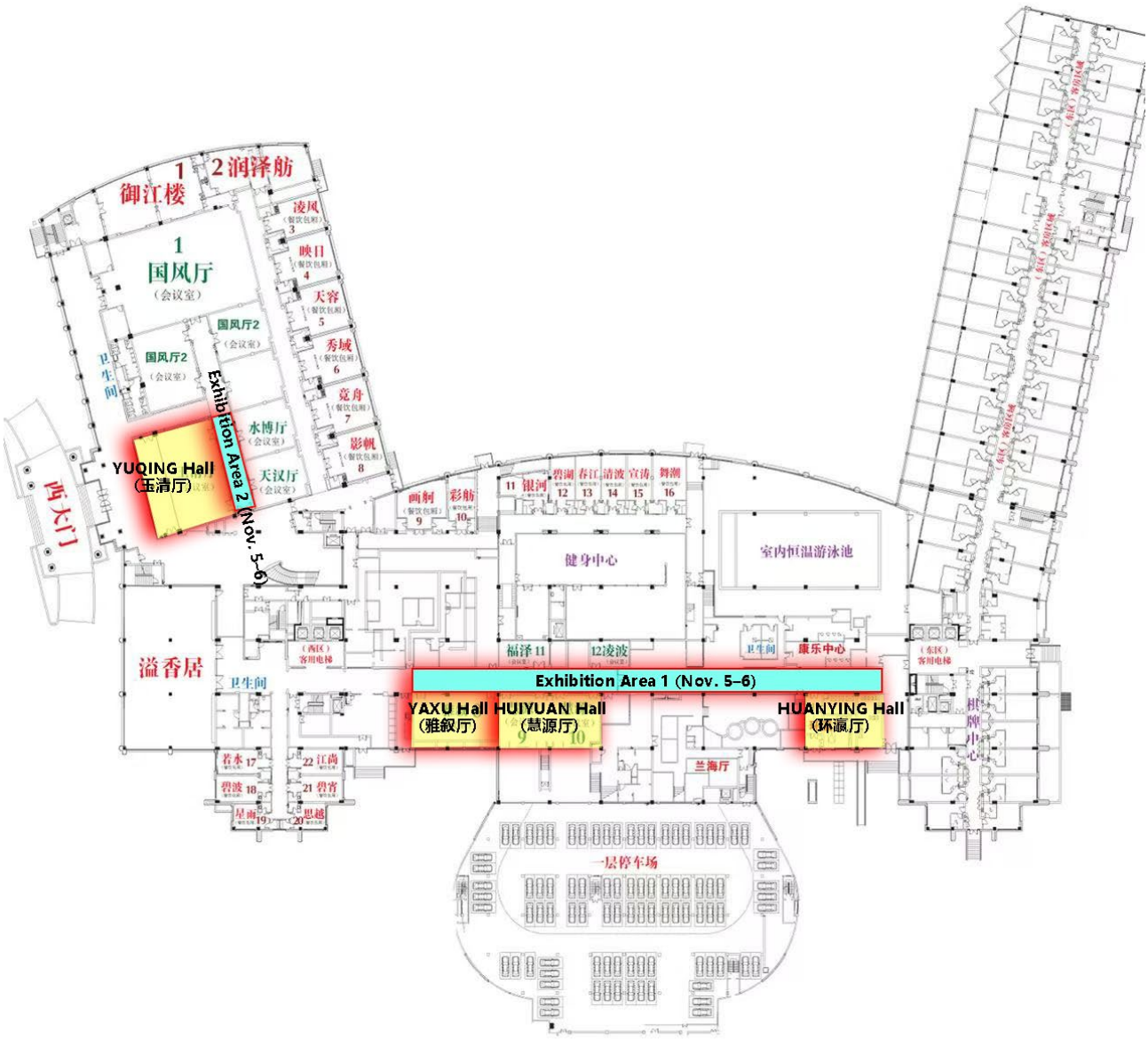
EXHIBITION HALL AND MEETING ROOMS

Opening Ceremony (开幕式及大会讲座)	BAOSHENG Hall @Level 2 (2 楼宝盛厅)
Parallel Sessions (分会场)	Room 1: HUANYING Hall @Level 1 (1 楼环瀛厅) Room 2: HUIYUAN Hall @Level 1 (1 楼慧源厅) Room 3: YAXU Hall @Level 1 (1 楼雅叙厅) Room 4: YUQING Hall @Level 1 (1 楼玉清厅) Room 5: QIER Hall @Zheda Yuanzheng International Hotel in Haining **(Round-trip shuttle service from Hangzhou provided)** (海宁浙大圆正国际酒店启尔厅，**提供杭州往返大巴接送**)

宝盛水博园大酒店(2F)平面图



宝盛水博园大酒店(1F)平面图



PROGRAM OVERVIEW

Symposium Web: https://wai-emc.com/wai2026/

Symposium Hours

November 4, 2026, 8:30 – 17:30

November 5, 2026, 8:40 – 18:00

November 6, 2026, 8:30 – 12:00

November 4 – Wednesday

- ☐ Official Opening and Keynote Speeches
- ☐ Industry Plenary
- ☐ Technical Exhibition

November 5 – Thursday

- ☐ Industry Plenary
- ☐ Oral Sessions
- ☐ Best Student Paper Competition
- ☐ Poster Discussion
- ☐ Young Professionals Forum
- ☐ Technical Exhibition
- ☐ Award Ceremony

November 6 – Friday

- ☐ Oral Sessions
- ☐ Technical Exhibition
- ☐ IBIS Summit China

2026 IEEE International Workshop on Advanced Interconnects
November 4-6, 2026

Date	Time	Agenda
Nov. 4th	08:30-09:00	**Opening Ceremony**
	09:00-12:00	**Keynote Speeches**
	12:00-13:40	**Lunch (Buffet)**
	14:00-15:30	**Industry Plenary**
	15:30-15:50	**Tea Break**
	15:50-17:30	**Industry Plenary**
	18:30	**Dinner (Buffet)**

2026 IEEE International Workshop on Advanced Interconnects
November 4-6, 2026

Date	Time	HUANYING Hall (环瀛厅)	HUIYUAN Hall (慧源厅)	YAXU Hall (雅叙厅)	YUQING Hall (玉清厅)	QIER Hall at Haining (Shuttle provided) (海宁圆正酒店启尔厅，杭州往返大巴接送)
Nov. 5th	8:40-10:20	*Industry Plenary*		*Best Student Paper Competition*		
	10:20-10:40	**Tea Break**				
	10:40-12:00	*Industry Plenary*		*Best Student Paper Competition*		
	12:00-13:30	**Lunch (Buffet) & Rest**				
	13:30-15:10	*[SS1] Electromagnetic Measurement and Near-Field-Based EMI Modeling*	*[SS2] Interconnect Reliability & Materials*	*Best Student Paper Competition*	*Poster Session*	*[SS3] Interconnect Characterization and Signal Integrity Analysis*
	15:10-15:30	**Tea Break**				
	15:30-16:30	*[SS4] Intelligent Parametric Modeling and Inverse Design of Microwave Components and Metasurfaces*	*[SS5] Advanced Printed Circuit Technologies at Millimeter-wave and Terahertz Technologies*	*Best Student Paper Competition*	*Poster Session*	*Young Professionals Forum*
	16:30-17:00					
	17:00-18:00					
	18:30	**Banquet Dinner & Award Ceremony**				
Nov. 6th	8:30-9:30	*[SS6] Signal Integrity and Equalization for AI and High-Speed Links*	*[SS7] Electromagnetic Measurement and Testing of Components and Systems*	*[SS8] Advanced Computational Algorithms and Multiphysics Modeling for Integrated Systems*	*IBIS Summit China*	
	9:30-10:30			*[SS9] AI-Assisted TCAD and EDA for Devices and Circuits*		
	10:30-10:50	**Tea Break**				
	10:50-12:00	*[SS10] Power Integrity and EMI Protection for Power Delivery Networks*	*[SS11] Physics-Based Modeling and Design Optimization of Interconnects and Wireless Systems*	*[SS12] Advanced Multiphysics Analysis and Coupled-Physics Mechanisms*	*IBIS Summit China*	
	END					

KEYNOTE SPEECH I

TITLE	**Progress and Challenges in SI/PI with AI/ML**
TIME	9:00 – 09:40, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	James L. Drewniak



ABSTRACT

Artificial Intelligence LLMs and Machine Learning algorithms have had a profound impact on progress in many areas of signal integrity and power integrity. However, significant challenges still remain in providing solutions to everyday SI/PI design problems. High-bandwidth memory, facilitated by the thru silicon via (TSV), and rapidly shrinking silicon feature sizes using innovative lithography technologies have given rise to GPU and memory advances enabling this new age of AI/ML. Many innovations in SI/PI are underway using AI/ML for everything from facilitating the productivity of experienced engineers, to addressing some common and significant design challenges. Examples will be given showing the power of AI for dramatically enhancing the productivity of experienced engineers. Progress in applying ML to solve some of the most difficult and time-consuming problems in SI/PI will also be presented. Finally, thoughts and perspectives on AI/ML directions in SI/PI will be discussed.

BIOGRAPHY

James L. Drewniak (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana Champaign, IL, USA, in 1985, 1987, and 1991, respectively. He is currently a Curator's Professor Emeritus with the Missouri University of Science and Technology (Missouri S&T), Rolla, MO, USA. His research interests include electromagnetic compatibility, signal and power integrity, and electronic packaging.

KEYNOTE SPEECH II

TITLE	**High-Speed Cable Backplane Systems for AI Infrastructure: Speed of light Challenges at 224G and 448G**
TIME	9:40 – 10:20, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Stephen Scearce



ABSTRACT

As AI training and inference clusters scale to unprecedented bandwidth requirements, cable backplane interconnects have become a critical bottleneck and enabler for next-generation system architectures. This presentation examines the engineering challenges of designing, qualifying, and deploying high-speed cable backplane systems at 224 Gb/s and emerging 448 Gb/s data rates for AI infrastructure. Topics include signal integrity considerations for copper twinax cable at extreme data rates (including PAM4/PAM6 modulation schemes), mechanical float and connector design for reliable high-density interconnects, system BERT-based qualification methodologies, and lessons learned from large-scale cartridge reliability programs. The talk will address the tradeoffs between insertion loss, reach, and manufacturability that engineering teams must navigate as the industry pushes toward higher bandwidth per lane, and will share practical approaches to qualification and reliability testing that support high-volume deployment in AI data center environments.

BIOGRAPHY

Stephen Scearce is Senior Director of Cable Backplane Systems at Amphenol Communications Solutions, leading a global engineering organization responsible for the AI industry's high-speed cable backplane interconnects at 224G and 448G data rates. With over 25 years of experience in signal integrity, power integrity, mechanical/thermal design, and high-speed hardware systems, his career spans NASA, Cisco Systems, and now Amphenol. He holds a B.S. in Engineering Technology and an M.S. in Electrical Engineering, both Summa Cum Laude, from Old Dominion University, and holds multiple U.S. patents in signal and power integrity, EMC and Mechanical design. He is a longtime volunteer with the IEEE EMC Society, currently serving as Finance Vice President and previously as co-chair of the IEEE EMC+SIPI 2025 Symposium in Raleigh, NC.

KEYNOTE SPEECH III

TITLE	**High Bandwidth Memory and Computing-in-memory Technology**
TIME	10:40 – 11:20, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Yimao Cai



ABSTRACT

As large language models become more widely used, optimizing their deployment for AI applications on edge devices has drawn growing attention. Edge devices impose strict requirements on processing speed, energy use, and computational stability. Traditional von Neumann architectures, which mainly rely on DRAM and HBM, struggle to meet these demands in edge settings. This talk will explore a compute-in-memory strategy based on 3D VNAND Flash. It aims to overcome the VNAND Flash memory wall and enable more efficient deployment of large language models on edge devices.

BIOGRAPHY

Cai Yimao, Dean of the School of Integrated Circuits, Boya Distinguished Professor, doctoral supervisor, and Executive Director of the Innovation Center for Advanced Integrated Circuits at Peking University. He is a recipient of the National Outstanding Youth Science Fund, and the Special Government Allowance of the State Council. He has long been engaged in research on memory and AI chips. He has directed a number of national-level projects including the National Key R&D Program and Key Programs of the National Natural Science Foundation of China. He developed novel RRAM memory and in-memory computing intelligent chips with practical applications. He has published more than 150 papers in top-tier conferences and journals including IEDM, VLSI, and Nature Electronics, with over 100 authorized Chinese patents.

KEYNOTE SPEECH IV

TITLE	**Signal and Power Integrity of Advanced Semiconductor Packaging in the AI Era**
TIME	11:20 – 12:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Seungyoung Ahn



ABSTRACT

As Moore's Law slows down, advanced semiconductor packaging of 2.5D and 3D heterogeneous integration has emerged as the paramount driver for next generation performance and miniaturization. However, this dense architectural evolution introduces unprecedented challenges, making Signal Integrity (SI) and Power Integrity (PI) critical bottlenecks for high speed, reliable system such as High-Bandwidth Memory (HBM).

Addressing these complex multiphysics hurdles requires a paradigm shift in design methodologies. This talk explores the current landscape and future trajectory of advanced packaging technologies, emphasizing SI/PI design management is essential for system performance mentioning the revolutionary role of Machine Learning (ML) in reshaping package design. By leveraging AI-driven optimization and automated co-design, engineers can drastically reduce time-to-market and navigate vast design spaces efficiently. We would like to discuss how the synergy of advanced packaging and AI will shape the future of high-performance computing.

BIOGRAPHY

Seungyoung Ahn received the B.S., M.S., and Ph.D. degrees from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1998, 2000, and 2005, respectively, in electrical engineering. From 2005 to 2009, he was a Senior Engineer with Samsung Electronics, South Korea, where he was the in charge of high-speed board design for laptop computer systems. He is currently a Professor with the CCS Graduate School of Mobility, KAIST, Daejeon. He has been working in the area of signal and power integrity, wireless power transfer, and electromagnetic compatibility design publishing 300+ international conference and journal papers. He was the Distinguished Lecturer of IEEE EMC Society and the recipient of several awards including Technical Achievement Award 2024 and Motohisa Kanda Award 2021 in IEEE EMC society.

INDUSTRY PLENARY I

TITLE	**Advanced Packaging SI/PI Analysis: Challenges, Methodologies, and EDA Practices**
TIME	14:00 – 14:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Yin Sun, DetoolTech Ltd, China



ABSTRACT

Advanced packaging is rapidly evolving toward higher integration, higher bandwidth, and higher power density, while increasingly complex power delivery networks and high-speed interconnects are introducing new challenges for signal and power integrity. This presentation focuses on key SI/PI challenges in advanced packaging, covering analysis methodologies from DC power integrity and AC impedance to high-speed channel analysis. Through practical application cases, we will demonstrate how EDA technologies can support SI/PI analysis, problem diagnosis, and design optimization in advanced packaging.

BIOGRAPHY

Dr. Yin Sun has extensive experience in EDA technology development and product planning, with a focus on advanced packaging, signal integrity, and power integrity analysis. She has extensive practical experience in SI/PI simulation, modeling, and signoff. In recent years, she has focused on electrical integrity analysis for 2.5D/3D packaging, chiplet-based systems, and high-speed interconnects, with a commitment to developing domestic SI/PI analysis and verification solutions for advanced packaging.

INDUSTRY PLENARY II

TITLE	**AI-Driven Heterogeneous 3D IC Stacking: Redefining Advanced Packaging at the Chip Level** **AI 驱动 3D IC 异构异质堆叠，重构 3D IC 先进封装产业芯层级**
TIME	14:30 – 15:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Alex Zhao, Zhuhai Silicon Chip Technology Ltd., China



ABSTRACT

The continued evolution of AI computing is driving chip systems toward higher bandwidth, greater integration density, and increasingly sophisticated heterogeneous integration. In 3D IC systems, chiplets based on different functions, process nodes, and even technology platforms are integrated through high-density interconnects and vertical stacking, extending the design scope from individual dies to cross-die, cross-layer system-level co-design. This evolution introduces not only increasing challenges in interconnect density, power consumption, and thermal management, but also increasingly complex coupling across system architecture, physical implementation, multi-physics simulation, and process technology. Faced with an enormous design space and multiple competing objectives, conventional design methodologies based on point tools and sequential iterations are encountering growing limitations.

In this presentation, Dr. Zhao Yi, General Manager of Zhuhai Silicon Chip Technology Ltd. (SiChip), will explore a new “AI + 3D IC EDA” design paradigm and discuss how AI can enable system-level collaborative design for heterogeneous 3D integration. By building an innovative toolchain for 3D IC design,

key stages across the entire workflow—including architecture design, physical implementation, multi-physics simulation, verification, and testing—can be seamlessly connected.
The presentation will further introduce the collaborative deployment of SiChip's 3D IC EDA AI Agent, Chips Z, together with the 3Sheng EDA platform. By integrating advanced packaging know-how with AI capabilities, the solution enables cross-layer data collaboration, design space exploration, and automated multi-objective iterative optimization, continuously driving the convergence of an end-to-end closed-loop System-Technology Co-Optimization (STCO) workflow. Through AI-driven transformation of 3D IC design methodologies, toolchains, and collaborative workflows, advanced packaging can evolve from isolated point innovations toward system-level innovation, opening up new possibilities and a higher level of innovation for the 3D IC industry.
AI 算力持续演进，正在推动芯片系统向更高带宽、更高集成度和更复杂的异构异质集成发展。面向 3D IC，不同功能、不同工艺节点乃至不同技术体系的 Chiplet 通过高密度互连与立体堆叠形成复杂系统，设计对象也由单一芯片进一步延伸至跨 Die、跨层级的系统协同。随之而来的，不只是互连密度、功耗与热等问题的叠加，更是架构、物理设计、多物理场仿真、工艺等环节之间日益复杂的耦合关系。面对庞大的设计空间和多目标约束，依赖单点工具与串行迭代的传统设计方式正面临新的挑战。本次演讲，硅芯科技总经理赵毅博士将围绕“AI+3D IC EDA”新设计范式，探讨如何以 AI 驱动异构异质堆叠下的系统级协同设计。通过构建面向 3D IC 的创新型工具链，贯通架构设计、物理实现、多物理场仿真、验证及测试等全流程关键环节。并通过硅芯科技 3D IC EDA AI Agent——Chips Z 及 3Sheng EDA 工具平台的协同实践，进一步融合先进封装 Know-how 与 AI 能力，实现跨层级数据协同、设计空间探索以及多目标自动迭代寻优，推动端到端 STCO 闭环持续收敛。以 AI 重塑 3D IC 设计方法、工具体系与协同流程，推动先进封装从单环节创新走向系统级创新，进一步打开 3D IC 产业新的“芯层级”。

BIOGRAPHY
Holding a Ph.D. from the University of Southampton, UK, under the supervision of Royal Society Fellow Professor Bashir Hashimi, he embarked on 2.5D/3D stacked IC design research in 2008 as part of one of the world's earliest pioneering research teams exploring advanced chip architecture methodologies, having collaborated with IMEC for 3D-IC technology validation. With 15 years of dedicated R&D in 3D integrated circuit design, he has published several excellent papers and awarded the VLSI-SOC Best Paper.
Currently serving as Founder and Chief Scientist at Zhuhai Silicon Chip Technology Ltd. , he has been a majority of leading national research initiatives. He directs the team in developing self-proprietary 2.5D/3D Stacked IC EDA tools, enabling critical advancements in the semiconductor industry through backend full-flow EDA tools and solutions.
英国南安普顿大学博士，师从英国皇家科学院院士（Prof Bashir Hashimi），2008 年投身 2.5D/3D 堆叠芯片设计研究，是当时世界最早期研究前沿芯片架构设计方法的研究团队之一，与 IMEC 完成 3D-IC 成果验证。深耕三维集成电路设计研发 15 年，发表多篇国际顶尖论文并获 VLSI-SOC 国际最佳论文。
现任珠海硅芯科技有限公司的创始人兼首席科学家，承担国家重点研发计划项目，带领团队自研 2.5D/3D 堆叠芯片 EDA 软件，以后端全流程 EDA 工具及解决方案推动芯片产业实现关键技术突破。

INDUSTRY PLENARY III

TITLE	**From Wafer to System: Advanced Packaging Solutions for Heterogenous Integration and Chiplets**
TIME	15:00 – 15:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Boping Wu, JCET Group Co., China



ABSTRACT

The end of conventional Dennard scaling and the rising cost of advanced node lithography have driven the semiconductor industry toward a paradigm shift: from monolithic System-on-Chip (SoC) to heterogeneous integration and chiplet-based architectures. This transition, however, places extreme demands on nanoscale fabrication, interfacial reliability, and system-level thermal-mechanical management—demands that cannot be met by traditional back-end packaging alone. In this talk, we present a comprehensive advanced packaging roadmap spanning from 2.5D interposer technologies to full 3D stacked systems, with an emphasis on the underlying nano-packaging science and manufacturing innovation.

We examine the technological landscape of 2.5D and 3D packaging solutions, comparing silicon interposers, organic interposers, and emerging bridge-die architectures in terms of electrical performance, thermal management, and cost efficiency. Particular emphasis is placed on through-silicon via (TSV) and through-glass via (TGV) technologies as critical enablers for vertical integration, addressing challenges in aspect ratio control, void-free filling, and reliability under thermal cycling.

A core contribution involves cross-scale thermomechanical modeling methodologies that bridge sub-micron structural mechanics with wafer-level warpage analysis. These finite element-based simulations enable predictive assessment of stress distributions in complex multi-material stacks, informing design rules for high-density interconnects.

To address the process complexity of conformal dielectric deposition in TSV/TGV structures, we introduce an AI+EDA co-optimization framework. Specifically, machine learning models are trained to predict and control ALD and CVD process parameters, reducing development cycles for ultra-thin barrier and seed layers critical for advanced packaging metallization. Experimental validation on a pilot line demonstrates that AI-optimized ALD reduces defect density by two orders of magnitude compared to conventional recipe-based approaches.

Finally, we discuss the integration roadmap toward full 3D chiplet stacking with nano-scale interconnects and emerging thermal interface materials. The talk concludes with a perspective on standardization needs (UCIe, BoW) and the role of nano-packaging in enabling domain-specific accelerators for AI, HPC, and photonic computing.

BIOGRAPHY

Dr. Boping Wu earned his Ph.D. in Electrical Engineering from the University of Washington, Seattle. He is currently Vice President of JCET Group and General Manager of the Technology Service Business Unit. Dr. Wu is an inventor on dozens of patents and author of numerous refereed publications on 3-D system integration and high speed interconnects. Over a 20-year career, he has led packaging R&D and product prototyping programs at various semiconductor companies, such as Philips, IBM, and Intel.

INDUSTRY PLENARY IV

TITLE	**Data Storage Innovations & Trends**
TIME	16:00 – 16:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Jianjun LUO, Hangzhou Dianzi University, China



ABSTRACT
Solid-State Drive (SSD) is rising to replace traditional hard drive (HDD) and flash memory becomes the most popular Non-Volatile memory in data storage industry. Supercomputing and AI demands greatly stimulated the storage technology development. It is facing challenge of higher density and performance as well as reliability when going to the next generation with the most advanced semiconductor process. Flash memory controller should take actions to clean the issues for the next generation Solid-State Drive with Flash Memory. At the same time, new memory devices, such as RRAM, MRAM and FeRAM, are exploring their niche market. However, these new memory technologies have to make trade-off to satisfy the unique applications. This key-note speech is going to allocate these memory devices in dedicated applications according to their advantages and disadvantages.

BIOGRAPHY
Jianjun (Jerome) Luo, the Dean of Microelectronic Research Institute in Hangzhou Dianzi University, also the founder and CTO of Sage Microelectronics. He earned a PhD in semiconductor material from Zhejiang University in China, a Master's in Microelectronics from the Hangzhou Dianzi University, and a Bachelor's in Electronics Engineering from Shanghai Jiaotong University. He founded Baleen Systems Inc in Silicon Valley in USA and started his new venture of Sage Micro in China since 2011, accumulated his experience in communication and storage IC design for more than 30 years. He won the 2nd Prize of National Scientific and Technological Progress Award, and Ho Leung Ho Lee Foundation's Scientific and Technological Award.

INDUSTRY PLENARY V

TITLE	**High-Speed Link Analysis Across Electrical and Optical Domains: Co-Simulation and Testing**
TIME	16:30 – 17:00, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Sun Anbing, Ruijie Networks, China



ABSTRACT
Growing bandwidth demand continues to push data rates higher. As a result, electrical channels face shorter practical reach and tighter design margins, driving wider use of optical links in high-speed systems. Retimed pluggables, LPO, NPO, and CPO represent different approaches to optical connectivity, each placing the boundary between the electrical and optical domains at a different point. The degree of separation between the two domains determines whether their impairments can be evaluated independently or must be considered at the system level. Drawing on a 112G application case, the presentation explores system-level electro-optic co-simulation and test design, including correlation between simulation and measurement, link budget allocation, and practical SI considerations. Beyond simulation and testing, the presentation discusses how signal integrity and optical engineering teams can combine system-level understanding with practical experience to guide system design and architecture decisions while methods and standards continue to evolve.

BIOGRAPHY
Sun Anbing is a senior hardware system engineer at Ruijie Networks. He joined ZTE in 2009, focusing on research in signal integrity / power integrity and having 16 years of experience in high speed core switch device development. He joined Ruijie Networks in 2020 and currently serves as a hardware system architecture engineer, leading the hardware system architecture design of next generation data center switches and research on new technologies.

INDUSTRY PLENARY VI

TITLE	**Interconnection & Simulation Techniques for Next-Generation NPO Switch**
TIME	17:00 – 17:30, November 4th
VENUE	BAOSHENG Hall @Level 2
SPEAKER	Rongyao Tang, FiberHome Telecommunication Technologies Co., Ltd, China



ABSTRACT
AI scale-up computing has driven the interconnect bottleneck off the die and onto in-cabinet channels, making copper-based electrical links impractical as lane rates move toward 200G. Near-package optics (NPO) offers a pragmatic engineering balance, capturing most of the signal-integrity benefits of co-packaged optics while preserving repairability and a conventional supply chain. This work presents a 51.2T NPO switch integrating sixteen 32 × 100G/3.2T optical engines, detailing flip-chip packaging, multi-physics system-technology co-optimization (STCO), and calibrated electrical-optical-electrical end-to-end simulation validated against hardware. We further discuss scalability to 6.4T/12.8T through advanced packaging and co-simulation.

BIOGRAPHY
Tang is the Staff Engineer and Interconnect Chief Expert at FiberHome, leading signal-integrity design of high-speed electro-optical channels in packages and PCBs, backed by 10+ years in high-speed design and an HUST optical/electronic background.

INDUSTRY PLENARY VII

TITLE	**Photonic Components and Packaging Technologies for Optical Interconnects**
TIME	8:40 – 9:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Torsten Wipiejewski, Huawei Technologies Duesseldorf GmbH, Munich, Germany



ABSTRACT
Optical interconnects have been used in data centers for many years. Connections lengths span from meters to several kilometers. For shorter distances inside racks electrical interconnects are typically used due to their lower cost. However, with speed levels going up, electrical interconnects become very lossy leading to high power consumption. Thus, optical interconnects are becoming attractive solutions when the electrical-optical interface can be placed close to the electronic chips. In co-packaged optics (CPO) the optical engine is directly integrated into the electrical chip package, whereas in near packaged optics (NPO) the optical engine comes in its own package and is placed next to the electronics chip. Several solutions exist including Si-photonics optical chips with external laser light sources or VCSEL based solutions for low cost packaging schemes. Another proposal is the deployment of many optical channels in parallel with relatively slow data rates per lane. In this case the optical medium plays an important role in terms of space

requirements and cost. Finally, it is the overall system that defines the most suitable solution in terms of performance, reliability and cost and also energy consumption.

BIOGRAPHY

Dr. Torsten Wipiejewski joined Huawei Technologies in 2014 and is responsible for the European technology sourcing of Huawei's Hardware Engineering Institute. His interest covers all hardware aspects for products ranging from smart watches to optical communication systems. Previously, Torsten was an investor in renewable energy, CEO at Optogan (Germany, Finland) making blue LEDs, and COO at Firecomms (Ireland) making optical transceivers for automotive and home networking applications. He also held management positions at ASTRI in Hong Kong, Agility Communications in Santa Barbara, CA, USA as well as Infineon, Osram, and Siemens in Germany. Torsten received a "summa cum laude" Ph.D. degree in electrical engineering from the University of Ulm, Germany and has been an executive member of several international conferences. He was the General Chair of ECTC2008 and has lectured several courses at conferences and universities. He holds more than 30 patents and has published over 100 scientific papers and presentations.

INDUSTRY PLENARY VIII

TITLE	**Emerging Trends and Challenges: System-Level Signal Integrity and Power Integrity/Delivery in the AI/SI Superchip Era**
TIME	09:10 – 09:40, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Kinger Cai, Arm Limited, USA



ABSTRACT

The rapid evolution of AI toward superintelligence is driving unprecedented growth in computing performance, memory bandwidth and capacity, high-speed interconnects, and power density. These trends introduce increasingly complex challenges in signal integrity (SI), power integrity (PI), power delivery, and thermal management across next-generation AI supercomputing platforms.

This presentation explores emerging architectures, including NVIDIA Vera Rubin and AMD Helios, and the evolution of memory technologies such as DDR, LPDDR, MRDIMM, SOCAMM, and HBM, alongside high-speed interconnects including PCIe, CXL, NVLink, UALink, and Ethernet. Key SI/PI challenges include channel loss, crosstalk, jitter, simultaneous switching noise, PDN impedance, voltage transients, and complex 3D packaging and interconnects.

The presentation highlights opportunities in advanced electromagnetic modeling, channel equalization, integrated system-level SI/PI co-design, optimized power delivery, liquid cooling, and comprehensive validation. It emphasizes that compute, memory, interconnects, power delivery, and thermal management must evolve together to enable scalable, energy-efficient, and reliable AI supercomputing infrastructure.

BIOGRAPHY

Kinger is Sr. Principal / Director driving Super AI platform electrical architecture design validation, & HVM, and advancing industry Power & Signal Integrity standards, in ARM.

Kinger was a Principal Engineer/Director in Intel, led cross-functional teams in AI PC coherent architecture strategies across CPU / GPU platforms and oversaw numerous SoC design & sign-off across mobile, client, discrete GPU, & CPU server products.

Kinger earned his Ph. D from Shanghai Jiao Tong University in 2001 and MBA degree from W.P. Carey business school in ASU in 2008.

Kinger is an IEEE Sr. Member, currently serves as Vice Chair in IBIS Open Forum.

Kinger has been focusing on signal & power integrity domains for 25+ years.

Kinger holds 14 granted patents, and published 30+ papers.

INDUSTRY PLENARY IX

TITLE	**M3EM Studio: High-Performance Electromagnetic Simulation for System-Level EMC/EMI Analysis**
TIME	09:40 – 10:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Li Xiang, Third Paradigm (Ningbo) Technology Co., Ltd. China



ABSTRACT

System-level electromagnetic compatibility (EMC) and electromagnetic interference (EMI) analysis requires efficient modeling of complex geometries and interactions between electromagnetic fields and circuits. This presentation introduces M3EM Studio, a high-performance electromagnetic simulation platform combining the time-domain finite integration technique (FIT), Advanced Conformal Enhancement (ACE) technology, and GPU acceleration. ACE improves the representation of geometric details and curved boundaries, while GPU acceleration enables efficient full-wave simulation of large-scale models. Synchronous and asynchronous field‑circuit co-simulation supports the coupled analysis of electromagnetic structures and circuit responses. Complementary macromodeling tools provide passivity, causality, and reciprocity assessment and correction, together with SPICE model generation for system-level simulation. Integrated preprocessing, postprocessing, and workflow automation support various applications. The presentation outlines the platform's numerical methods and computational capabilities, with an emphasis on electromagnetic coupling, interference assessment, and EMC-oriented design.

BIOGRAPHY

Li Xiang is currently the Product Director at Third Paradigm (Ningbo) Technology Co., Ltd., where he leads the product definition of M3EM Studio, a GPU-accelerated full-wave electromagnetic simulation software for system-level EMC/EMI analysis. He has nearly a decade of industry experience spanning EMC simulation, device modeling, and IC design. Prior to joining Third Paradigm, he was an EMC Expert at Huawei, where he was deeply involved in the EMC design of several best-selling digital products, and later worked at Nano Core Chip (NCC), a Hangzhou-based AI chip company, where he led on-chip ESD protection design for multiple mass-production ICs. He received the Master's degree from Zhejiang University, Hangzhou, China, in 2018.

INDUSTRY PLENARY X

TITLE	**Next-Generation Modular Ethernet Switches: Challenges and Trade-offs in High-Speed Internal Interconnects**
TIME	10:40 – 11:10, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Siyuan Yang, Cisco, China



ABSTRACT

This presentation explores the critical demands of AI data centers on modular Ethernet switches and their high-speed internal interconnects. Driven by rapidly increasing bandwidth requirements, modern switches face major complexities, including large chip packaging, ultra-high power consumption, and high-speed SerDes that make internal interconnect design highly challenging. Using a comparative case study of major Cisco switching platforms, this session delivers a clear analysis of PCB backplanes, direct orthogonal connections, and cable backplanes across key trade-offs: channel loss, cost, reliability, and serviceability. Ultimately, this talk provides practical architectural frameworks and engineering insights to guide the reliable design of next-generation switching systems.

BIOGRAPHY
Siyuan Yang is a Principal Engineer and Hardware R&D Manager at the Cisco China Research and Development Center. In this dual leadership role, he manages the hardware engineering team for enterprise core switches while simultaneously directing the architecture design for Cisco's next-generation modular platforms. With over 20 years of deep industry expertise, he has successfully delivered numerous enterprise modular switches and some AI data center switching platforms. He graduated with a Master's degree from Beihang University (BUAA) in 2003.

INDUSTRY PLENARY XI

TITLE	**Power Rail Coupling and Its Impact on High-Speed Signals Across Die-Package-PCB**
TIME	11:10 – 11:40, November 5th
VENUE	HUANYING Hall @Level 1
SPEAKER	Yajun Zhang, Sanechips Technology Co., Ltd. (ZTE Microelectronics), China



ABSTRACT
With the explosive growth of artificial intelligence (AI) applications and the evolution of wireless communication toward higher-order modulation schemes, the performance requirements for RF systems have become increasingly stringent. Power coupling noise—including both power-to-power coupling and power-to-signal coupling—directly degrades these performance metrics, and the resulting error vector magnitude (EVM) degradation is significantly amplified under high-order modulation. Consequently, RF systems place demanding requirements on the optimization of power noise, particularly coupling noise, in both PCB and package designs. Currently, high-speed analog IP vendors typically rely on frequency-domain isolation metrics to constrain PCB and package design. However, such conventional isolation metrics have limitations and can even mislead design practices. To address these challenges, this talk proposes a full-link simulation methodology that combines frequency-domain transfer impedance analysis with time-domain coupling analysis, enabling more efficient optimization of power-to-power coupling and power-to-signal coupling. Using a practical flip-chip project as a case study, the methodology is applied to achieve co-design for suppressing noise coupling from die and package to PCB, covering the complete workflow from modeling and simulation to coupling localization.

BIOGRAPHY
Zhang Yajun is a Senior PI/SI Engineer at Sanechips Technology Co., Ltd. (ZTE Microelectronics). He graduated from Shandong University and previously worked at Huawei Technologies Co., Ltd. HiSilicon Semiconductor Business Department. He is engaged in full-link PI/SI simulation and testing at chip and package level, and has 10 years of experience in high-speed circuit PI/SI design.

OVERVIEW OF BEST STUDENT PAPER COMPETITION

VENUE	YAXU Hall (雅叙厅)
TIME	8:40-16:30 November 5th
FINALISTS	
8:40-8:55	**No.1 A 0.1-0.84 GHz Bandpass Filter with Reconfigurable Frequency, Bandwidth and Multiple Transmission Zeros (#1571354398)** *Mingye Shi, Zhen Tian and Sheng Wang (National Key Laboratory of Electromagnetic Space Cognition Technology, China); Xu Zhu (University. of Electronic Science and Technology.of China, China)*
8:55-9:10	**No.2 A Hybrid PEEC-FEM Framework for Two-Way Electrothermal Analysis of Planar Transformers (#1571350995)** *Hangkai Zhang (Zhejiang University); Xu Wang (DeTooLIC Technology Co., China); Bo Pu and Yanwu Wang (DeTooLIC Ltd. Technology, China); Xinglin Sun (Zhejiang University, China)*
9:10-9:25	**No.3 A General Peeling Algorithm Based on Conductor and Dielectric Losses Compensation for Impedance Reconstruction (#1571353594)** *Jiyang Liu, Zi-Xi Chen, Si-Yao Tang and Xing-Chang Wei (Zhejiang University, China)*
9:25-9:40	**No.4 Pre-Layout Case Study of Lateral and Vertical Power Delivery Using PDN Shape Synthesis (#1571345363)** *Ruiqi Dai, Haran Manoharan and Suho Lee (Missouri University of Science and Technology, USA); Kundan Chand and Grace Yu (Meta Platforms, USA); Chulsoon Hwang (Missouri University of Science and Technology, USA)*
9:40-9:55	**No.5 Quantum-Kernel Residual Regression for Metal Contacts to β-Ga2O3 (#1571354187)** *Qi Shen, Jintang Wang, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)*
9:55-10:10	**No.6 Agent-Guided Iterative Signal-Integrity Design: PCIe 6.0 and DDR5 Case Studies (#1571357515)** *Qiuhong Ye, Jienan Chen and Kuo Liao (University of Electronic Science and Technology of China, China)*
10:40-10:55	**No.7 Signal Integrity Analysis of Narrowband near-Field Communication Links Based on Low-Frequency Magnetoelectric Mechanical Antennas (#1571356416)** *Shizhan Jiang (Chongqing University, China); Ruixin Xu (Chongqing university, China); Wei Zhou (Chongqing University, China); Zhaoqiang Chu (Harbin Engineering University, China); Da Yi and Ming-Chun Tang (Chongqing University, China)*
10:55-11:10	**No.8 Multiharmonic Spatiotemporal Modulation for Crosstalk Control in Coupled Transmission Lines (#1571353809)** *Kishwar Ali (University of Aquila, Italy); Ayesha Shabbir, Giulio Antonini and Daniele Romano (University of L'Aquila, Italy); Martin Štumpf (VUT, Czech Republic); Elia Mattucci and Petr Kadlec (Brno University of Technology, Czech Republic); Francesco Ferranti (Luleå University of Technology, Sweden); Jonas Ekman (Lulea University of Technology, Sweden)*
11:10-11:25	**No.9 Efficient via Placement Optimization for Irregular Power Distribution Network Using Deep Reinforcement Learning (#1571365891)** *Junjie Ren, Ling Zhang, Li Jiang, Keyi Ding, Chenxu Zhang and Er-Ping Li (Zhejiang University, China)*

11:25-11:40	**No.10 Real-Time Dynamic Magnetic Hysteresis Compensation in TMR Sensors Using Point-by-Point Inverse PI Model (#1571350699)** *Tianhao Pan, Jun Wang and Xing-Chang Wei (Zhejiang University, China)*
11:40-11:55	**No.11 Three-Dimensional SAR Reconstruction from Two-Plane Electric-Field Measurements Using Numerical Green's Functions (#1571355763)** *Zhelun Chen and Xing-Chang Wei (Zhejiang University, China)*
13:30-13:45	**No.12 Macrobending Loss in Single-Mode Fibers: Comparison of Analytical and Full-Vector Finite-Element Models (#1571347175)** *Zanyu Xu and Xing-Chang Wei (Zhejiang University, China)*
13:45-14:00	**No.13 Construction of a Repeatable 6G-Oriented Channel Model in a Reverberation Chamber (#1571353916)** *Boyan Zhang, Tian Zhou, Sen Zhang and Yuan Zhao (Chengdu University of Information Technology, China)*
14:00-14:15	**No.14 A Hybrid Finite Element Physics-Informed Neural Network Framework for Electromagnetic-Thermal Analysis (#1571354929)** *Qingnan Fan, Yijie He and Huan Huan Zhang (Xidian University, China)*
14:15-14:30	**No.15 Inductance Modeling of Inclined Bond Wires with Finite Length and Return Path Effects (#1571351112)** *Xiaoya Zhou (Beijing University of Posts and Telecommunications, China); Dan Shi (Beijing University of Posts and Telecommunications, China); Yanchi Liu (Beijing University of Posts and Telecommunications, China); Peng Zhang (State Radio Regulation Committee, China); Jinde Wang and Machen Yin (Beijing University of Posts and Telecommunications, China)*
14:40-14:55	**No.16 Stacking-Dependent Dipole Engineering of Metal/β-Ga2O3 Contacts with Atomically Thin h-BN Interlayers (#1571353696)** *Tianyu Lin and Wenjie Yin (National University of Defense Technology, China); Zhiqiang Fan (Changsha University of Science and Technology, China); Yuxiong Long and Jiayu Dai (National University of Defense Technology, China)*
14:55-15:10	**No.17 A qNEHVI-Based Bayesian Optimization Framework for Ku-Band Hairpin Filter Design (#1571353429)** *Yuhao Pan, Junhan Huang and Liang Chen (Shanghai University, China)*
15:30-15:45	**No.18 A Physics-Driven Deep Finite Element Method for Fast Electro-Thermal Analysis of 3D Interconnects (#1571345974)** *Yijie He, Qingnan Fan, Huan Huan Zhang, Bian Wu and Ying Liu (Xidian University, China)*
15:45-16:00	**No.19 An Absorption Spectrum is Not a Thermometer (#1571365587)** *Kun-Lai Li (Beihang University); Weikang Si (National Institute of Metrology, China); Rui-Yun Liu, Zhengpeng Wang, Yongjun Xie, Tao Zhang and Xiangxuan Feng (Beihang University, China)*
16:00-16:15	**No.20 Per-Frequency Relative-Gain Self-Calibration for Sequential Sphere-Scan Quiet-Zone Reconstruction (#1571365646)** *Rui-Yun Liu and Zhiping Li (Beihang University, China); Kun-Lai Li (Beijing University of Aeronautics and Astronautics, China); Weikang Si (National Institute of Metrology, China)*
16:15-16:30	**No.21 A Wideband Hollow Rectangular Dielectric Waveguide Antenna for Sub-THz Wireless Interconnect Applications (#1571358228)** *Changsheng Sun and Xiaochun Li (Shanghai Jiao Tong University, China); Haibing Zhan (Hunan Institute of Engineering, China); Ken Ning (Shenzhen University, China)*

TITLE	**A 0.1-0.84 GHz Bandpass Filter with Reconfigurable Frequency, Bandwidth and Multiple Transmission Zeros**
TIME	8:40-8:55, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHOR	Mingye Shi, Zhen Tian and Sheng Wang (National Key Laboratory of Electromagnetic Space Cognition Technology, China); Xu Zhu (University. of Electronic Science and Technology.of China, China)

ABSTRACT
This paper presents a lumped-element bandpass filter (BPF) with simultaneously reconfigurable center frequency (CF), bandwidth, and transmission zeros (TZs). Hybrid couplings with inductive-dominant and capacitive-dominant coupling are adopted in the main coupling path, so that the TZs move synchronously with the tuning of frequency and bandwidth, ensuring good out-of-band rejection. The bandwidth is tuned by the coupling capacitors, the CF tuned by the resonator capacitors, and two SP4T switches connect four tunable filters to form an ultra-wide-tuning-range filter bank. A prototype covering 0.1-0.84 GHz with a fractional bandwidth (FBW) of 10%-20% is fabricated; the rejection at points offset by 25% from the passband edge is better than 30 dBc.

TITLE	**A Hybrid PEEC-FEM Framework for Two-Way Electrothermal Analysis of Planar Transformers**
TIME	8:55-9:10, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Hangkai Zhang (Zhejiang University); Xu Wang (DeTooLIC Technology Co., China); Bo Pu and Yanwu Wang (DeTooLIC Ltd. Technology, China); Xinglin Sun (Zhejiang University, China)

ABSTRACT
Planar-transformer electrothermal modeling is challenging due to complex multiscale geometries and frequency-dependent winding losses. This paper presents an efficient hybrid PEEC--FEM framework using independent electromagnetic and thermal meshes. PEEC predicts the winding inductance and losses without meshing the surrounding air and dielectric regions, while FEM solves the thermal problem on a coarse cuboidal mesh. Electromagnetic losses are transferred to the thermal mesh, and the computed temperature is mapped back to update the temperature-dependent copper conductivity, enabling two-way coupling. For a 3-D planar transformer operating at 300kHz, the proposed method shows close agreement with an independent full-FEM multiphysics model, with differences of 0.016\% in total loss and 2.7\% (0.79K) in peak temperature rise. The coupled solution converges within nine iterations, with a loss-transfer error below 0.071\%.

TITLE	**A General Peeling Algorithm Based on Conductor and Dielectric Losses Compensation for Impedance Reconstruction**
TIME	9:10-9:25, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Jiyang Liu, Zi-Xi Chen, Si-Yao Tang and Xing-Chang Wei (Zhejiang University, China)

ABSTRACT
For lossy and nonuniform transmission lines, distributed transmission-line loss decreases the accuracy of time domain reflectometry (TDR) based impedance reconstruction. This paper proposes a general loss-compensated peeling algorithm, which models each transmission line section with both conductor loss (series resistance) and dielectric loss (shunt conductance). A recursive procedure is then developed to compensate for these two loss mechanisms. This method is verified by numerical simulations and measurements. In the measurement, the proposed method reduces the mean absolute error of the transmission line impedance from 3.682 Ω to 0.397 Ω, corresponding to an accuracy improvement of 89.2%.

TITLE	**Pre-Layout Case Study of Lateral and Vertical Power Delivery Using PDN Shape Synthesis**
TIME	9:25-9:40, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Ruiqi Dai, Haran Manoharan and Suho Lee (Missouri University of Science and Technology, USA); Kundan Chand and Grace Yu (Meta Platforms, USA); Chulsoon Hwang (Missouri University of Science and Technology, USA)

ABSTRACT
With increasing power density and integration complexity, modern power delivery network (PDN) design is moving from conventional lateral power delivery toward more vertical delivery. In a PDN layout, the power delivery path from the source to the load is shaped by the power plane topology, layer transitions, and stackup. This paper presents a pre-layout case study of lateral and vertical power delivery under different ball grid array (BGA) ball placement options, evaluating the resulting synthesized PDN shapes and DC resistance (DCR). PMIC BGA ball locations are varied while the SoC BGA pins are kept fixed, producing multiple source placement candidates for each delivery case. For each candidate placement, the synthesis flow using reinforcement learning generates a power plane shape, and a resistance engine based on physical modeling evaluates the DCR. The results show clear changes in the synthesized multilayer PDN geometry and DCR with different PMIC placements in both delivery cases. The DCR results show a consistent trend that the vertical cases generally have lower DCR than the lateral cases over many of the evaluated placements.

TITLE	**Quantum-Kernel Residual Regression for Metal Contacts to β-Ga2O3**
TIME	9:40-9:55, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Qi Shen, Jintang Wang, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)

ABSTRACT
Metal contacts to β-Ga2O3 are governed by interface-specific bonding, band bending, gap states, and tunneling, making work-function screening unreliable. We combine density functional theory and nonequilibrium Green's function calculations with quantum-kernel residual regression for small-sample metal screening. For 13 metals at an n-type doping concentration, the selected model gives a post-selection leave-one-metal-out root-mean-square error of 0.5645 decades, a coefficient of determination of 0.9811, and 89.7 percent pairwise ranking accuracy, with lower internal-benchmark error than seven conventional regressors. Atomistic transport analysis is then used to interpret and verify prioritized candidates.

TITLE	**Agent-Guided Iterative Signal-Integrity Design: PCIe 6.0 and DDR5 Case Studies**
TIME	9:55-10:10, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Qiuhong Ye, Jienan Chen and Kuo Liao (University of Electronic Science and Technology of China, China)

ABSTRACT
We present an expert-supervised agent workflow for iterative signal-integrity design, combining constrained geometry actions, simulation feedback, and reusable tool refinement. PCIe 6.0 results show worst package transmission of −3.8 dB at 16 GHz and four lane error counts of 3, 2, 2, and 4 in a channel annotated with 32-dB loss. DDR5 read/write eyes are evaluated at 8000 Mb/s with two ranks. The case studies illustrate the workflow; agent-specific gains require controlled comparisons.

TITLE	**Signal Integrity Analysis of Narrowband near-Field Communication Links Based on Low-Frequency Magnetoelectric Mechanical Antennas**
TIME	10:40-10:55, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Shizhan Jiang (Chongqing University, China); Ruixin Xu (Chongqing university, China); Wei Zhou (Chongqing University, China); Zhaoqiang Chu (Harbin Engineering University, China); Da Yi and Ming-Chun Tang (Chongqing University, China)

ABSTRACT
The signal integrity of a narrowband near-field magnetoelectric (ME) mechanical antenna communication link is experimentally investigated. The link exhibits a −3 dB bandwidth of approximately 800 Hz near 36.5 kHz, corresponding to a fractional bandwidth of about 2.2%. At 20 Vpp, square-wave tests reveal a waveform-transition rate near 500 bps, beyond which the steady-state plateau disappears and the pulse amplitude progressively decreases. At 2000 bps, the pulse amplitude decreases to approximately 50% of its low-rate value. ASK experiments at 100, 500, and 2000 bps show progressively reduced eye opening and stronger attenuation of off-resonance spectral components. These results establish a direct relationship between the narrowband frequency response and time-domain waveform distortion, providing an experimental basis for near-field communication-link evaluation and waveform compensation.

TITLE	**Multiharmonic Spatiotemporal Modulation for Crosstalk Control in Coupled Transmission Lines**
TIME	10:55-11:10, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Kishwar Ali (University of Aquila, Italy); Ayesha Shabbir, Giulio Antonini and Daniele Romano (University of L'Aquila, Italy); Martin Štumpf (VUT, Czech Republic); Elia Mattucci and Petr Kadlec (Brno University of Technology, Czech Republic); Francesco Ferranti (Luleå University of Technology, Sweden); Jonas Ekman (Lulea University of Technology, Sweden)

ABSTRACT
This work introduces a multiharmonic state-space coupled-mode theory (SS-CMT) for coupled energy analysis in distributed space--time-modulated transmission lines. We model the underlying periodic variation in mutual inductance and capacitance through duty-cycle-controlled, step-like traveling-wave modulation. Unlike sinusoidal modulation, a step-like waveform couples the excitation signal to multiple Floquet sidebands, allowing coupled energy to be redistributed away from the excitation (fundamental) frequency. We use the proposed SS-CMT to compute the main-line through response, near-end and far-end crosstalk, validated with a 1-D FDTD solver. Our results show that appropriate modulation parameters reduce crosstalk components at the excitation frequency by modifying duty-cycle-dependent DC components and redirecting energy toward Floquet sidebands, while considerably enhancing the main-line output through energy exchange with the modulation source/pump.

TITLE	**Efficient via Placement Optimization for Irregular Power Distribution Network Using Deep Reinforcement Learning**
TIME	11:10-11:25, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Junjie Ren, Ling Zhang, Li Jiang, Keyi Ding, Chenxu Zhang and Er-Ping Li (Zhejiang University, China)

ABSTRACT
This paper proposes a novel deep reinforcement learning (DRL) framework for via placement optimization in irregular power distribution network (PDN). A modified Double Dueling Deep Q-Network (D3QN) with an adaptive via-budget constraint is developed to efficiently explore the large combinatorial design space. The

reward function combines target-impedance improvement with via-count penalties. To support fast PDN impedance evaluation, a pattern-based analytical method (PBM) is employed to assess the impact of via placement changes. Experimental results on an irregular multilayer PDN demonstrate that the proposed method achieves the target impedance with fewer vias while maintaining comparable computational efficiency to representative optimization methods. The optimized impedance profile also shows close agreement with full-wave simulation.

TITLE	**Real-Time Dynamic Magnetic Hysteresis Compensation in TMR Sensors Using Point-by-Point Inverse PI Model**
TIME	11:25-11:40, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Tianhao Pan, Jun Wang and Xing-Chang Wei (Zhejiang University, China)

ABSTRACT
Tunnel Magnetoresistance (TMR) sensors offer ultra-high sensitivity but suffer from severe nonlinear magnetic hysteresis, degrading measurement accuracy in dynamic (AC) magnetic fields. Traditional compensation methods based on the Prandtl-Ishlinskii (PI) inverse model generally rely on static zero-point averaging, rendering them ineffective for continuous AC signal correction. This paper proposes a system-level dynamic compensation method that extends the PI inverse model to a point-by-point real-time mapping strategy. A fully automated software-hardware system is developed, executing pre-cycle magnetic flushing, data acquisition, parameter identification, and real-time compensation at a high sampling rate of 10,240 Hz. Experimental validations under 1 Hz and 52 Hz triangular wave magnetic fields demonstrate that the proposed method tightly tracks the ideal linear response. It significantly reduces the Root Mean Square Error (RMSE) by up to 51%, proving its effectiveness for high-precision dynamic magnetic field measurement.

TITLE	**Three-Dimensional SAR Reconstruction from Two-Plane Electric-Field Measurements Using Numerical Green's Functions**
TIME	11:40-11:55, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Zhelun Chen and Xing-Chang Wei (Zhejiang University, China)

ABSTRACT
A three-dimensional specific absorption rate reconstruction method based on numerical Green's functions and planar equivalent Hertzian dipole sources is proposed. Electric-field data on two observation planes are used to recover the equivalent source distribution through differential evolution, after which the volumetric electric field and peak one gram SAR are reconstructed. The method is validated at 2.45 GHz using a half-wave dipole and an elliptical loop antenna, with additional intermediate planes used for independent field validation. The overall one gram SAR distribution errors are 2.38 percent and 7.53 percent, while the corresponding peak one gram SAR errors are 0.64 percent and 2.71 percent. The results demonstrate the effectiveness of the proposed method for three-dimensional SAR reconstruction from limited planar field measurements.

TITLE	**Macrobending Loss in Single-Mode Fibers: Comparison of Analytical and Full-Vector Finite-Element Models**
TIME	13:30-13:45, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Zanyu Xu and Xing-Chang Wei (Zhejiang University, China)

ABSTRACT
Conventional macrobending-loss analysis often assumes an infinite cladding and therefore neglects reflections at the finite cladding-coating interface. This work develops two-dimensional axisymmetric finite-element models for a weakly guiding step-index single-mode fiber at 1550 nm. An infinite-cladding approximation and a coated-fiber model are compared with the Marcuse, Renner, and Faustini formulas. Under the infinite-cladding approximation, Marcuse and COMSOL show nearly identical exponential trends, with a log-loss

correlation coefficient of 0.999869, although Marcuse gives 16%-72% higher losses. The maximum difference between the two orthogonal polarization branches is only 0.424%. With the coating, the simulated loss shows clear oscillation and polarization splitting. Renner and Faustini reproduce the increase in peak spacing with bend radius; their maximum deviations in mean peak spacing are 4.4% and 1.1%, respectively. However, both show systematic peak shifts and amplitude errors. Thus, Marcuse is useful for trend estimation, whereas the coated-fiber formulas are mainly useful for estimating the oscillation period. Accurate loss values require a full-vector model with realistic boundaries.

TITLE	**Construction of a Repeatable 6G-Oriented Channel Model in a Reverberation Chamber**
TIME	13:45-14:00, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Boyan Zhang, Tian Zhou, Sen Zhang and Yuan Zhao (Chengdu University of Information Technology, China)

ABSTRACT
Wireless-device testing for sixth-generation systems must balance channel-propagation fidelity against experimental reproducibility. In this paper, a method is proposed for constructing and reproducibly recreating an indoor channel model for sixth-generation systems in a reverberation chamber. By loading the cavity with absorbing materials, the propagation state is tuned, and the Rician factor and the root-mean-square delay spread are investigated over the 2 to 6 gigahertz band as two metrics characterizing the channel state. The results show that loading the absorbers markedly raises the Rician factor over the whole band and reduces the root-mean-square delay spread, shifting the channel from a strongly reverberant state toward a more pronounced line-of-sight-dominated state. This work demonstrates that, once the reverberation chamber is calibrated, a saved configuration can be recalled to repeatedly reproduce the target sixth-generation indoor channel, providing a feasible platform for reproducible wireless-device testing.

TITLE	**A Hybrid Finite Element Physics-Informed Neural Network Framework for Electromagnetic-Thermal Analysis**
TIME	14:00-14:15, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Qingnan Fan, Yijie He and Huan Huan Zhang (Xidian University, China)

ABSTRACT
With the rapid development of high-frequency and high-power microwave technologies, accurate and efficient electromagnetic-thermal simulation of microwave devices has become increasingly important. In this paper, a hybrid finite element physics-informed neural network framework is proposed for electromagnetic-thermal analysis of microwave devices. For the electromagnetic analysis, the Helmholtz equation is discretized using the finite element method, and the resulting finite element equations are incorporated into the neural network through a physics-informed residual loss to obtain the electromagnetic field. The power dissipation density calculated from the electromagnetic field is then introduced into the thermal model as the heat source. For the thermal analysis, the steady-state heat conduction equation is discretized using the finite element method, and the corresponding finite element variational functional is employed as the training objective of the thermal network. In this manner, the electromagnetic and thermal fields are solved within a unified hybrid finite element physics-informed neural network framework. An H-plane bend waveguide is investigated as a representative microwave device to demonstrate the effectiveness of the proposed approach.

TITLE	**Inductance Modeling of Inclined Bond Wires with Finite Length and Return Path Effects**
TIME	14:15-14:30, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Xiaoya Zhou (Beijing University of Posts and Telecommunications, China); Dan Shi (Beijing University of Posts and Telecommunications, China); Yanchi Liu (Beijing University of Posts and Telecommunications, China); Peng Zhang (State Radio Regulation Committee, China); Jinde Wang and Machen Yin (Beijing University of Posts and Telecommunications, China)

ABSTRACT
This paper presents a local inductance model for finite inclined bond wires. The model uses local height, inclination angle, and distance to the nearest endpoint to calculate the wire inductance for a specified return path. Local height and endpoint distance are parameterized by arc length. A smooth minimum combines the geometric scale associated with the wire and ground plane with a finite length scale, and the resulting inductance per unit length is integrated along the wire. A reference model is constructed using quasistatic electromagnetic extraction with a continuous ground plane and return terminals located at the projections of the wire endpoints. The dataset comprises seven inclination angles, seven lengths, and eight frequencies, giving 392 data points. Data at angles from 0 to 60 degrees are used for parameter calibration, data at 75 degrees are used for parameter selection, and data at 85 degrees are reserved for independent testing. Across the 56 independent test data points, the proposed model achieves a mean absolute error (MAE) of 0.0021 nH and a mean absolute percentage error (MAPE) of 0.6848%. These results support the accuracy of the proposed model for finite inclined bond wires under the tested geometric and return path conditions.

TITLE	**Stacking-Dependent Dipole Engineering of Metal/ β -Ga2O3 Contacts with Atomically Thin h-BN Interlayers**
TIME	14:40-14:55, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Tianyu Lin and Wenjie Yin (National University of Defense Technology, China); Zhiqiang Fan (Changsha University of Science and Technology, China); Yuxiong Long and Jiayu Dai (National University of Defense Technology, China)

ABSTRACT
Metal-semiconductor contacts are critical electrical interfaces in advanced interconnects, where precise barrier control must be balanced against efficient current transmission. For β -Ga_2O_3, interface states [1] and metal-induced gap states [2] can constrain Schottky barrier engineering. Here, we investigate atomically thin hexagonal boron nitride (h-BN) interlayers as a means of tailoring Ag/ β -Ga_2O_3 contact transport through stacking-dependent interfacial dipoles [3,4].First-principles quantum-transport calculations are performed for four contact configurations: a bare Ag/ β -Ga_2O_3 interface, a monolayer h-BN interlayer, and AB- and BA-stacked bilayer h-BN interlayers. The bilayer configurations maintain identical composition and layer count while reversing the stacking-associated out-of-plane dipole [5,6], enabling a controlled comparison of stacking-dependent transport. The calculated currents span up to about 7 orders of magnitude across the investigated configurations and biases. Monolayer h-BN suppresses the current by approximately one order of magnitude relative to the bare contact while yielding an approximately exponential forward-bias response with a thermionic-equivalent ideality factor of 2.12. It favors forward rectification, whereas the bilayer interlayers exhibit the opposite rectification polarity. Notably, AB stacking produces currents 10-20 times higher than BA stacking at each of the 12 sampled biases. Spatially resolved local-density-of-states analysis is consistent with a lower interfacial transport barrier in the AB configuration, supporting a dipole-mediated interpretation of the transport contrast.These results identify h-BN stacking and its associated out-of-plane dipole as additional design variables for engineering β -Ga_2O_3 contacts without changing interlayer composition or thickness. The findings also reveal a trade-off between barrier modulation and interlayer-induced current suppression, providing atomistic guidance for metal-semiconductor interface design relevant to advanced interconnects.

TITLE	**A qNEHVI-Based Bayesian Optimization Framework for Ku-Band Hairpin Filter Design**
TIME	14:55-15:10, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Yuhao Pan, Junhan Huang and Liang Chen (Shanghai University, China)

ABSTRACT
High-fidelity optimization of compact microwave filters is computationally expensive because of strongly coupled geometric variables and competing electrical objectives. This article presents a synthesis-informed Bayesian optimization-HFSS (BO-HFSS) workflow for a fifth-order Ku-band microstrip hairpin filter. Six symmetry-reduced variables are optimized using Gaussian-process surrogates, q-noisy expected hypervolume improvement (qNEHVI), and two-level probability-of-feasibility screening. BO is compared with NSGA-II and simulated annealing using the same full-wave model, constraints, 16.0-16.4-GHz passband, and 200-evaluation budget. BO identifies 14 strictly feasible and 180 relaxed-feasible designs, compared with 9/146 for NSGA-II and 13/174 for simulated annealing. It also finds its first strictly feasible design after only 14 evaluations, whereas the baselines require 51 and 45 evaluations. These results demonstrate that BO produces a high-quality feasible Pareto set with fewer expensive full-wave simulations.

TITLE	**A Physics-Driven Deep Finite Element Method for Fast Electro-Thermal Analysis of 3D Interconnects**
TIME	15:30-15:45, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Yijie He, Qingnan Fan, Huan Huan Zhang, Bian Wu and Ying Liu (Xidian University, China)

ABSTRACT
As interconnect dimensions shrink, voltage drop, Joule heating, and temperature rise become increasingly significant, making rapid electro-thermal analysis of 3D interconnects essential. Based on the deep finite element method (DFEM), we use mesh node coordinates as network inputs and nodal potential or temperature rise as outputs, and construct an energy-type loss function from discrete physical matrices. Validation on a double-layer orthogonal interconnect model with four M1 lines, four M2 lines, and six vias shows that the electric potential network achieves a relative L2 error of 1.25% on conductor nodes; The temperature network achieves a relative L2 error of 0.09% over all nodes and 0.03% on conductor nodes. Total runtime is 26.82 s versus 171 s for COMSOL, with peak CPU memory of 1.12 GB and GPU memory of 26 MB, compared with 2.09 GB for COMSOL. The proposed method thus reduces computation time by 84.3% and CPU memory by 46.4%, while maintaining high field prediction accuracy.

TITLE	**An Absorption Spectrum is Not a Thermometer**
TIME	15:45-16:00, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Kun-Lai Li (Beihang University); Weikang Si (National Institute of Metrology, China); Rui-Yun Liu, Zhengpeng Wang, Yongjun Xie, Tao Zhang and Xiangxuan Feng (Beihang University, China)

ABSTRACT
Identical absorption spectra can conceal different thermal responses. For reflected structures in a perfectly conducting cavity under fixed symmetric excitation and common thermal conditions, we derive a sharp pairwise minimax relative error bound for predictions using only the spectrum. For steady conduction with constant thermal conductivity, uniform convection on one face, and insulation elsewhere, absorbed power and the first spatial moment of the heat source exactly determine the mean temperature rise on the opposite face. Three-dimensional finite-difference time-domain (FDTD) and heat conduction simulations yield a mean temperature rise ratio of 3.84 and a 58.7% bound in the discrete model. The first-moment method evaluates this mean without solving for the temperature field.

TITLE	**Per-Frequency Relative-Gain Self-Calibration for Sequential Sphere-Scan Quiet-Zone Reconstruction**
TIME	16:00-16:15, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Rui-Yun Liu and Zhiping Li (Beihang University, China); Kun-Lai Li (Beijing University of Aeronautics and Astronautics, China); Weikang Si (National Institute of Metrology, China)

ABSTRACT
Relative-gain mismatch degrades quiet-zone reconstruction from sequential perfect electric conductor (PEC) sphere scans. This paper presents per-frequency self-calibration using known co-polarized Mie transfer functions. The estimator alternates between noise-weighted Tikhonov reconstruction and closed-form gain updates. Generalized cross-validation selects the regularization parameter, and no cross-frequency smoothing is applied. Paired simulations across 30 randomized scenes over 8-13 GHz yield a mean spectral normalized mean-square error (NMSE) of −40.182 dB and, for rectangular PEC plates, a mean radar cross section (RCS) illumination-correction root-mean-square error of 0.0461 dB. Spectral NMSE improves by 4.74 and 22.56 dB over reference-sphere-only and uncalibrated three-sphere inversions, respectively. At equal per-channel signal-to-noise ratio and measurement budget, repeated-sphere comparisons detect no statistically significant radius-diversity benefit.

TITLE	**A Wideband Hollow Rectangular Dielectric Waveguide Antenna for Sub-THz Wireless Interconnect Applications**
TIME	16:15-16:30, November 5th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Changsheng Sun and Xiaochun Li (Shanghai Jiao Tong University, China); Haibing Zhan (Hunan Institute of Engineering, China); Ken Ning (Shenzhen University, China)

ABSTRACT
The hollow rectangular dielectric waveguide (HRDW) is an emerging low-loss and wideband sub-THz interconnect that has not yet been explored for antenna design. An HRDW antenna excited by a metallic waveguide transition is proposed in this paper. It operates from 181 to 294 GHz with a reflection coefficient below −10 dB, corresponding to an impedance bandwidth (IBW) of 47.6%. In addition, an average radiation efficiency of 89.3% and a maximum gain of 15.7 dBi are obtained. It also exhibits stable radiation patterns across the operating frequency range, with half-power beamwidths (HPBWs) of 16.4° and 16.0° in the H- and E-planes, respectively, at 240 GHz. The HRDW antenna also exhibits good main-beam symmetry and is compatible with printed circuit board (PCB) fabrication processes. With its wide bandwidth and high gain, the HRDW antenna shows potential for sub-THz wireless interconnect applications.

OVERVIEW OF SESSION I

SESSION	SS1 Electromagnetic Measurement and Near-Field-Based EMI Modeling
VENUE	HUANYING Hall (环瀛厅)
TIME	13:30-15:05 November 5th
SESSION CHAIRS	Da Yi, Chongqing University Pei Xiao, Hunan University Xing-Chang Wei, Zhejiang University
TECHNICAL TALKS	
13:30-13:50	**The Development Trend of Electromagnetic Safety in Integrated Circuits (#1571348874 Invited)** *Zhaowen Yan, Jianhao Ge, Fuyu Zhao and Siyuan Ma (Beihang University, China)*
13:50-14:05	**Reflection Loss of an EM Absorber from One-Port and Two-Port Free-Space Measurements (#1571345783)** *Branimir Pejcinovic and Ha Tran (Portland State University, USA); Adithya S. Ramachandran, Kent Thompson and Robert L. Doneker (TangiTek, LLC, USA)*
14:05-14:20	**New Fast System-Level EMI Simulation Method - Reverberant and Direct Field (#1571353960)** *Weitao Dai and Paul Bremner (RobustPhysics, USA)*
14:20-14:35	**Co-Simulation of Electromagnetic Fields and Cable Networks for Signal Integrity in Noisy Environments (#1571353963)** *Weitao Dai and Paul Bremner (RobustPhysics, USA)*
14:35-14:50	**Radial-Loaded Concentric-Arc Planar Sensor for Partial Discharge Detection: 1.5-3 GHz Receiving- Response Simulation (#1571360315)** *Jiyang Zhang, Pei Xiao and Gaosheng Li (Hunan University, China)*
14:50-15:05	**Broadband EMI Suppression Mechanism of an Asymmetric Hybrid Inductor (#1571347908)** *JinLiang Wang, Jinling Zhang and ShuangQing Xiong (Beijing University of Posts and Telecommunications, China)*

TITLE	**The Development Trend of Electromagnetic Safety in Integrated Circuits (Invited)**
TIME	13:30-13:50, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Zhaowen Yan, Jianhao Ge, Fuyu Zhao and Siyuan Ma (Beihang University, China)



ABSTRACT

This report focuses on the electromagnetic safety issues faced by integrated circuits in complex electromagnetic environments, and explores the importance of accurately obtaining the electromagnetic boundaries of integrated circuits and achieving forward-looking design. The report introduces precision detection techniques for electromagnetic emission, electromagnetic sensitivity, and electromagnetic vulnerability of integrated circuits, and also elaborates on modeling methods for conducted emission, near-field radiation emission, conducted sensitivity, and electromagnetic vulnerability of integrated circuits. This report points out that precise testing methods and devices for obtaining electromagnetic parameters of integrated circuits, integrated circuit electromagnetic compatibility modeling methods based on test results, and protection design methods based on integrated circuit electromagnetic compatibility models are the future development directions of integrated circuit electromagnetic safety research.

BIOGRAPHY

Zhaowen Yan received the B.S. degree, the M.S. degree and the Ph.D degree in electrical engineering from Henan Polytechnic University, Xi’an University of Science and Technology and Xi’an Jiaotong University, China, in 1991, 1996 and 1999, respectively. From 1999 to 2002 he was a Post-Doctoral Research Associate at the Huazhong University of Science and Technology. From April 2003 to May 2005, he hold a PostDoctorial position at Beihang University. From December 2012 to December 2013, he is a visiting scholar in EMC Laboratory, Missouri University of Science and Technology, U.S.A.

He is now a professor of electronic science and technology at Beihang University. For many years, his research activity was focused on the electromagnetic field computation and EMC analysis. He has published over 150 conferences and journal papers and 8 monographs on electromagnetic theory. He has 41 authorized patents. He won the first prize of the Natural Science of the Ministry of Education of PRC in 2003 and the first prize of National Defense Science and Technology Progress in 2011 as recognition of his research work. And the project he held won the second prize for the National Science and Technology Progress in 2012. He also won the first prize for National Defense Technology Invention in 2017. He won the first prize of the National Technology Invention in 2018.

TITLE	**Reflection Loss of an EM Absorber from One-Port and Two-Port Free-Space Measurements**
TIME	13:50-14:05, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Branimir Pejcinovic and Ha Tran (Portland State University, USA); Adithya S. Ramachandran, Kent Thompson and Robert L. Doneker (TangiTek, LLC, USA)

ABSTRACT

The reflection loss (RL) of a metal-backed absorber can be measured directly in a one-port configuration or calculated from free-standing two-port S-parameters by terminating the second port analytically. The two measurement approaches are similar but there are subtle differences in handling of the calibration reference planes. We compare both approaches on the same multi-layered silicone absorber, measured at four sample rotations with a 2-18 GHz bi-static spot-probe fixture. With the proper treatment of the calibration reference planes the two routes agree to 3.8 dB RMS over 8-18 GHz, vs. 8.7 dB with no de-embedding. A geometric constraint on the de-embedding distances, recovered from unconstrained fits, independently confirms the reference-plane model. Better agreement will be possible with an improved sample holder.

TITLE	**New Fast System-Level EMI Simulation Method - Reverberant and Direct Field**
TIME	14:05-14:20, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Weitao Dai and Paul Bremner (RobustPhysics, USA)

ABSTRACT

A fast system-level EMI simulation method is developed for multiply connected reverberant enclosures. Statistical power-balance equations determine the ensemble-averaged field levels, while electromagnetic reciprocity calculates cable and receiver responses. Deterministic direct-field interactions are added to recover location-dependent effects. The mesh-free formulation is computationally efficient, and comparisons with measurements show good agreement.

TITLE	**Co-Simulation of Electromagnetic Fields and Cable Networks for Signal Integrity in Noisy Environments**
TIME	14:20-14:35, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Weitao Dai and Paul Bremner (RobustPhysics, USA)

ABSTRACT
A co-simulation method is presented for evaluating signal integrity (SI) under reverberant-field electromagnetic interference (EMI). An EMI coupling calculation based on electromagnetic topology (EMT) predicts the nonstationary voltage induced in an interconnect within reverberation chambers (RCs), while a transmission-line model propagates a pseudorandom binary sequence (PRBS) through the interconnect. Their statistically rigorous combination predicts eye diagrams and bit error rate (BER). A USB cable example shows good agreement with measurements.

TITLE	**Radial-Loaded Concentric-Arc Planar Sensor for Partial Discharge Detection: 1.5-3 GHz Receiving- Response Simulation**
TIME	14:35-14:50, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Jiyang Zhang, Pei Xiao and Gaosheng Li (Hunan University, China)

ABSTRACT
A compact 50 mm × 50 mm concentric-arc planar sensor for electromagnetic partial-discharge (PD) detection is numerically investigated. Two symmetric diagonal branches are introduced as a radial-loading modification without changing the footprint. CST time-domain simulations over 0.01-8 GHz show that the dominant S11 minimum shifts from 4.17279 to 4.08490 GHz and changes from −33.38 to −56.28 dB. To evaluate receiving behavior independently of input matching, a controlled three-port microstrip-line fixture is used with the sensor board parallel to the excitation-line substrate and separated by an approximately 2 mm air gap. In the 3-5.5 GHz interval, the baseline sensor exhibits a −73.59 dB coupling null at 3.526 GHz, whereas the loaded sensor gives −44.06 dB at the same frequency and its deepest null is −57.55 dB at 3.845 GHz. At 4.0849 GHz, S12 increases locally by about 2.38 dB. The results show that radial loading shifts the resonance and suppresses or relocates selected receiving-response cancellations, but does not produce a uniform broadband gain.

TITLE	**Broadband EMI Suppression Mechanism of an Asymmetric Hybrid Inductor**
TIME	14:50-15:05, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	JinLiang Wang, Jinling Zhang and ShuangQing Xiong (Beijing University of Posts and Telecommunications, China)

ABSTRACT
This paper investigates the broadband suppression mechanism of an asymmetric air-core/ferrite hybrid inductor used in the LC filter of a microwave oven magnetron. The hybrid inductor is wound continuously from a single wire: one section is wound around a NiZn ferrite core, and the other is an air-core section without any magnetic core, the two sections being connected in series. Comparative one-port impedance and two-port transmission measurements of four cut-and-separated samples show that the ferrite-loaded section and the air-core section dominate EMI suppression in the low- and high-frequency bands, respectively. In the mid-frequency band, the ferrite-loaded section acts as a lossy load that damps the intrinsic resonance of the air-core section, so that the intact inductor maintains effective suppression over 30 MHz-1 GHz. Full-wave simulations based on a Lorentzian magnetic-dispersion model confirm these key features. Whole-system tests show that, with the hybrid inductor installed, the maximum radiated emission of the microwave oven over 30 MHz-1 GHz is reduced from about 92 dB μ V/m to below 45 dB μ V/m.

OVERVIEW OF SESSION II

SESSION	SS2 Interconnect Reliability & Materials
VENUE	HUIYUAN Hall (慧源厅)
TIME	13:30-15:15 November 5th
SESSION CHAIRS	Haohui Long, Shanghai Jiao Tong University Yunwen Wu, Shanghai Jiao Tong University
TECHNICAL TALKS	
13:30-13:50	**Fine Pitch RDL Interconnection on Glass Substrates: Materials, Interfaces, and Reliability (Invited)** *Wei Koh (Pacrim Technology, USA)*
13:50-14:10	**Reliability simulation and modeling for advance package processing (Invited)** *Dr. Qing Peng (IC Research Technology (WuHan) Co. LTD, China)*
14:10-14:30	**Reliability Study on Flexible Glass and Glass-Based Packaging Technology (Invited)** *Dr. Yang JinFa (TriumphScience&Technology Flexible Display Materials Co., Ltd., China)*
14:30-14:45	**Interconnection Mechanisms and Electromigration Reliability of Nanotwinned Copper Pillars for Advanced Packaging** *Dr. Zicheng Sa (Harbin Institute of Technology, China)*
14:45-15:00	**Study on Process Control of Low-Temperature, Low-Pressure Cu-Cu Bonding Using Perpendicular Nanotwinned Copper (#1571371211)** *Zihao Xiang (Shanghai Jiaotong University, China); Xingya Pan and Haohui Long (Shanghai Jiao Tong University, China); Xiaoqin Zeng and Yunwen Wu (Shanghai Jiaotong University, China)*
15:00-15:15	**Transient in-Plane Temperature Nonuniformity and Microbump Defects During Thermocompression Bonding of Multi-Chiplet Packaging (#1571359625)** *Wang Hexin (Central South University, China); Yiou Qiu (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Zimeng Guo (Central South University, China); Zhen Liu and Qiaobo Dai (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Chen Zhuo and Wenhui Zhu (Central South University, China)*

TITLE	**Fine Pitch RDL Interconnection on Glass Substrates: Materials, Interfaces, and Reliability (Invited)**
TIME	13:30-13:50, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Wei Koh (Pacrim Technology, USA)



ABSTRACT

A review of current trends in high-performance advanced packaging for AI/HPC, focus on heterogeneous integration enabling technologies: advanced fine-pitch, high-density RDL on glass substrates, 2.5D interposer packaging (CoWoS, CoPoS), 3D TSV HBM stacking roadmap, hybrid bonding, and outlook of TGV glass technology on packaging integration.

BIOGRAPHY

Dr. Wei Koh is an expert in microelectronics assembly and semiconductor packaging technology with over 40-year experience. He received the Bachelor of Science in Chemical Engineering from the University of Washington, followed by MS and PhD degrees in Chemical Engineering from Cornell University. He has held technical and leadership roles at Occidental Research Corp., Aerospace Electronics, Henkel Electronics Materials, Motorola Corporate Research, and Kingston Technology, with research spanning glass-ceramic through-hole (TGV) interposers,

IC packaging materials and memory chip packaging including HBM and USB NAND storage devices. He has pioneered in the development of flip chip bonding technology, Ball Grid Array (BGA) and Chip Scale Packaging (CSP), TGV interposer/glass substrate fabrication, and advanced high-density 3D IC multichip modules (MCM) with over 100 publications and 40 US patents. He is a Fellow of IEEE EPS Society.

TITLE	**Reliability simulation and modeling for advance package processing (Invited)**
TIME	13:50-14:10, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Dr. Qing Peng (IC Research Technology (WuHan) Co. LTD, China)

ABSTRACT
Reliability modeling and simulation in semiconductor manufacturing and packaging have become an important research direction in electronic manufacturing technology, with significant implications for economic development and national security. This talk will report the technologies and case studies developed at IC Research Technology (Wuhan) Co., Ltd. for reliability modeling and simulation in semiconductor chip manufacturing and packaging processes. The topics include computational lithography, thin-film growth, crystal growth, hybrid bonding, chemical mechanical polishing (CMP), molding, underfill curing, wire bonding, and reliability simulation. The progress and prospects of our proprietary industrial software, as well as its role in the electronic manufacturing field, will also be discussed.

BIOGRAPHY
Dr. Qing Peng is the Chief Scientist at IC Research Technology (Wuhan) Co., Ltd., China, and a Professor at Wuhan University. His long-term research focuses on the development and application of first-principles-based cross-scale and multiscale computational simulation algorithms. He has established a variety of cross-scale and multiscale computational models to investigate mechanical behavior under unconventional environments—including large strain, high temperature, high pressure, impact, intense irradiation, and stress corrosion cracking—with particular emphasis on reliability simulation and modeling for advanced electronic packaging. He received his B.S. degree from Peking University in 1998 and his Ph.D. degree from the University of Connecticut in 2005. He has published more than 300 SCI-indexed papers and has been listed among the World's Top 2% Scientists.

TITLE	**Reliability Study on Flexible Glass and Glass-Based Packaging Technology (Invited)**
TIME	14:10-14:30, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Dr. Yang JinFa (TriumphScience&Technology Flexible Display Materials Co., Ltd., China)

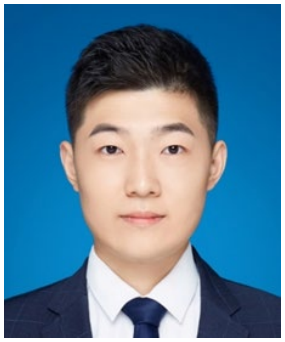


ABSTRACT
Flexible glass is a key material enabling foldable displays, wearable devices, and emerging electronic products. Technically, significant advances have been achieved in bendability, surface hardness, and optical transmittance. Industrially, the secondary thinning route represented by ultra-thin flexible glass (UTG) has reached mass production, with yield and cost remaining the primary constraints. Applications are expanding from foldable smartphones to foldable laptops, wearables, and aerospace flexible solar wings. Building on this, the application of glass is further extending into semiconductor packaging: glass substrates based on through-glass via (TGV) technology meet the requirements of Chiplet and HBM packaging, and the industry is transitioning from validation to volume production. Advancing materials and precision processing, and strengthening supply-chain collaboration and domestic substitution, constitute the core path toward self-reliant development of high-end displays and high-end chips.

BIOGRAPHY

Yang Jinfa, Professor-level Senior Engineer. For more than a decade, he has been devoted to the frontline of advanced glass new materials. He focuses on conquering core "bottleneck" technologies, realizing independent controllability and commercialization of multiple key technologies, advancing the upgrading of the display glass industry and safeguarding the security of industrial and supply chains. His honors include China Good Person, Anhui Most Outstanding Grassroots College Graduate, Bengbu Model Worker. He is a member of the National Outstanding Engineer Team, a talent recognized by the MIIT for advanced manufacturing technologies, and the lead of an Anhui provincial industrial innovation team.

TITLE	**Interconnection Mechanisms and Electromigration Reliability of Nanotwinned Copper Pillars for Advanced Packaging**
TIME	14:30-14:45, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Dr. Zicheng Sa (Harbin Institute of Technology, China)



ABSTRACT

Continued miniaturization of interconnects and increasing operating current densities in advanced packaging pose reliability challenges, including interfacial Kirkendall voids and electromigration-induced failure. This presentation focuses on microstructural control, interfacial reactions, and electromigration reliability in nanotwinned copper pillar interconnects. It introduces a direct-current electrodeposition method for fabricating nanotwinned copper pillars with a preferred (111) orientation and examines interfacial reactions in nanotwinned Cu/Sn solder joints. The effects of functional coatings on elemental diffusion, interfacial microstructure, and the mechanical properties of the joints are then discussed. Finally, electromigration in copper pillar solder joints under high current densities is examined, with particular attention to the mechanisms of atomic migration, interfacial segregation, and void evolution under the combined effects of electron wind force and microstructure. These studies can provide a theoretical basis and practical guidance for process development, materials design, interface optimization, and reliability enhancement in high-density copper pillar interconnects.

BIOGRAPHY

Zicheng Sa is an Associate Researcher in the School of Materials Science and Engineering at Harbin Institute of Technology. His research focuses on interconnect materials and reliability in advanced electronic packaging, with particular emphasis on three-dimensional (3D) chiplet packaging, heterogeneous integration, and the reliability and failure mechanisms of interconnect structures. He has participated in projects supported by the Key Program of the National Natural Science Foundation of China (NSFC), the Yeqisun Joint Fund, and the National Key Research and Development Program of China. He has published nine SCI-indexed papers in journals including Journal of Materials Science & Technology (JMST) and Journal of Materials Research and Technology (JMRT), as well as six EI-indexed papers. He has filed four patent applications, two of which have been granted.

TITLE	**Study on Process Control of Low-Temperature, Low-Pressure Cu-Cu Bonding Using Perpendicular Nanotwinned Copper**
TIME	14:45-15:00, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Zihao Xiang (Shanghai Jiaotong University, China); Xingya Pan and Haohui Long (Shanghai Jiao Tong University, China); Xiaoqin Zeng and Yunwen Wu (Shanghai Jiaotong University, China)



ABSTRACT

Cu Cu direct bonding is a core enabling technology for high density advanced 3D packaging. In this work, perpendicular nanotwinned Cu (p ntCu) with dense (110) texture was fabricated by additive controlled electrodeposition with optimized Cl^- concentration and current density. High quality low void bonding interfaces were achieved at 200 ° C, 1 MPa for 60 min, accompanied by obvious cross interface atomic diffusion. Further extending bonding time to 120 min at 2 MPa induces grain coarsening over 50 μm. This low temperature and low pressure bonding exhibits good process compatibility for 3D integration, providing a microstructure tuning strategy for low temperature Cu Cu bonding.

BIOGRAPHY

Dr. Zihao Xiang is an Assistant Researcher at the School of Materials Science and Engineering, Shanghai Jiao Tong University. He received his B.S. degree in 2016 and Ph.D. degree in 2022 from the University of Electronic Science and Technology of China. His research interests primarily focus on electrodeposition and advanced packaging technologies. He has published more than 10 SCI-indexed journal papers.

TITLE	**Transient in-Plane Temperature Nonuniformity and Microbump Defects During Thermocompression Bonding of Multi-Chiplet Packaging**
TIME	15:00-15:15, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Wang Hexin (Central South University, China); Yiou Qiu (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Zimeng Guo (Central South University, China); Zhen Liu and Qiaobo Dai (Changsha Anmuquan Intelligent Technology Co., Ltd., China); Chen Zhuo and Wenhui Zhu (Central South University, China)

ABSTRACT

Multi-chiplet packages impose increasingly stringent requirements on temperature uniformity and deformation control in microbump arrays during thermocompression bonding (TCB). In-plane temperature gradients induced by rapid localized heating have been shown to affect solder melting, wetting, and joint formation. However, for large-format packages with spatially nonuniform material distributions, the transient evolution of the temperature field within the microbump array and its relationship to bonding defects remain unclear. In this study, a two-dimensional transient heat transfer model of the microbump region was developed based on thermal resistance analysis, and a thermal simulation method employing region-specific equivalent material properties was proposed. The analytical and simulation results were validated through process optimization experiments using the Taguchi method. The results identify the nonuniform distribution of high-thermal-conductivity materials as the primary contributor to in-plane temperature gradient within the microbump array of the investigated package. During heating, these temperature gradient increase the risk of solder bridging in higher-temperature regions and incomplete bonding in lower-temperature regions; during cooling, they alter the local thermal deformation and stress distributions, making peripheral microbumps more susceptible to fracture. Process optimization reduced the peak in-plane temperature gradients from 301K to 215K, thereby mitigating these defects. These findings provide guidance for improving temperature uniformity and optimizing TCB process parameters in such packages.

OVERVIEW OF SESSION III

SESSION	SS3 Interconnect Characterization and Signal Integrity Analysis
VENUE	**Venue: Qier Hall, Haining Yuanzheng Hotel** **Round-trip shuttle service will be provided. The shuttle will depart from the Hangzhou Blossom Water Museum Hotel at approximately 12:30 PM on November 5, after lunch, and return to Hangzhou after the session for the conference banquet that evening.** **地点：海宁圆正酒店启尔厅** **会议提供往返大巴接送。大巴将于 11 月 5 日午餐后约 12:30 从杭州宝盛水博园大酒店出发，活动结束后返回杭州，参加当晚的大会晚宴。**
TIME	13:30-14:45 November 5th
SESSION CHAIRS	Ping Li, University of Electronic Science and Technology of China Xiaochun Li, Shanghai Jiao Tong University Min Tang, Shanghai Jiao Tong University
TECHNICAL TALKS	
13:30-13:45	**Double-Sides Launch Point Impedance Drift Correction for Accurate PCB Characteristic Impedance Measurement (#1571323552)** *Wai Hong Chee (Keysight Technologies, Inc., Malaysia); Brian Chi (Keysight Technologies, Taiwan); Eason Yang (Keysight Technologies, Inc., Taiwan)*
13:45-14:00	**Design and Tolerance Analysis of Differential Transmission Structures for High Speed Connectors (#1571367249)** *Lei Deng (LinkE Technologies, China); Lidong Cai (New H3C Technologies Ltd., China); Licheng Li (New H3C Technologies Ltd, China); Chaoqiang Zang (HUNAN University, China); Yinzhu Tang (Southwest University of Science and Technology, China); Chi Lidong (Hunan University, China); Yihong Qi (unknown)*
14:00-14:15	**Decomposition of Far-End Crosstalk in a Memory Channel (#1571364440)** *Wenzhi Wang and Qihang Shang (DeTooLIC Ltd. Technology, China)*
14:15-14:30	**UCIe Link Compliance Analysis in a Multi-Functional S-Parameter Post-Processing Platform (#1571364857)** *Zhifei Xu and Yajun Chen (DeTooLIC Ltd. Technology, China)*
14:30-14:45	**A Harmonic-Domain Electrical Modeling Framework for EMC and SI/PI Analysis (#1571347048)** *Alessandro Sona and Federico Tramarin (University of Padova, Italy)*

TITLE	**Double-Sides Launch Point Impedance Drift Correction for Accurate PCB Characteristic Impedance Measurement**
TIME	13:30-13:45, November 5th
VENUE	QIER Hall, Haining Yuanzheng Hotel
AUTHORS	Wai Hong Chee (Keysight Technologies, Inc., Malaysia); Brian Chi (Keysight Technologies, Taiwan); Eason Yang (Keysight Technologies, Inc., Taiwan)

ABSTRACT

Time Domain Reflectometry (TDR) and Vector Network Analyzer (VNA) measurements are widely used for characteristic impedance verification in printed circuit board (PCB) manufacturing. However, long transmission lines often exhibit an apparent impedance rising-slope effect that introduces measurement uncertainty and can lead to inaccurate impedance assessment. This phenomenon is primarily caused by the combined effects of dielectric loss, multiple reflections, and signal attenuation along the transmission path. As industry requirements evolve from ± 10% to ± 5% impedance tolerance specifications, improved measurement accuracy becomes increasingly important for manufacturing quality control.

This paper analyzes the physical mechanisms responsible for impedance drift in lossy transmission lines and proposes a double-sided launch-point compensation method. The technique utilizes TDR measurements

performed from both ends of the transmission line, aligns the spatial coordinates of the two profiles, and applies a weighted compensation algorithm that prioritizes the impedance information closest to each launch location. Experimental results demonstrate significant reduction of artificial impedance slope while preserving actual impedance discontinuities and physical variations. The method improves compliance evaluation against tight impedance specifications and has potential applications in high-volume PCB manufacturing environments.

TITLE	**Design and Tolerance Analysis of Differential Transmission Structures for High Speed Connectors**
TIME	13:45-14:00, November 5th
VENUE	QIER Hall, Haining Yuanzheng Hotel
AUTHORS	Lei Deng (LinkE Technologies, China); Lidong Cai (New H3C Technologies Ltd., China); Licheng Li (New H3C Technologies Ltd, China); Chaoqiang Zang (HUNAN University, China); Yinzhu Tang (Southwest University of Science and Technology, China); Chi Lidong (Hunan University, China); Yihong Qi (unknown)

ABSTRACT
High speed connectors require impedance control within limited channel dimensions and practical manufacturing tolerances. This paper presents a controlled comparison of edge and broadside coupled rectangular differential contacts inside a rectangular shielding cavity. Cavity dimensions, contact thickness, center to center spacing, and material properties are held fixed, while the nominal contact widths are adjusted to obtain nearly equal differential impedances. Cross sectional analysis relates width induced impedance variations to changes in the intercontact gap, facing surface width, and contact to shield coupling. When both contacts undergo the same width deviation within ± 20 μm, broadside coupling reduces the maximum absolute impedance deviation from 4.37 to 3.87 Ω, corresponding to an 11.4% reduction. Modal comparisons at the nominal geometries also show that significant transmission of the first higher-order differential mode begins at a higher frequency for broadside coupling. These results provide guidance for selecting connector transmission structures that improve robustness to contact width variations while accounting for modal behavior within a fixed channel envelope.

TITLE	**Decomposition of Far-End Crosstalk in a Memory Channel**
TIME	14:00-14:15, November 5th
VENUE	QIER Hall, Haining Yuanzheng Hotel
AUTHORS	Wenzhi Wang and Qihang Shang (DeTooLIC Ltd. Technology, China)

ABSTRACT
Link decomposition analysis quantifies how individual signal paths contribute to the overall channel response. This work decomposes the far-end crosstalk (FEXT) of a memory channel with ten coupled data lines into path contributions. Three mechanisms are identified: near-end crosstalk combined with reflection produces strong FEXT, longer paths produce delayed responses, and coupled vias partially cancel FEXT. These insights can guide design optimization and failure analysis.

TITLE	**UCIe Link Compliance Analysis in a Multi-Functional S-Parameter Post-Processing Platform**
TIME	14:15-14:30, November 5th
VENUE	QIER Hall, Haining Yuanzheng Hotel
AUTHORS	Zhifei Xu and Yajun Chen (DeTooLIC Ltd. Technology, China)

ABSTRACT
UCIe (Universal Chiplet Interconnect Express) is an open, multi-protocol die-to-die interconnect standard for multi-die packages. Verifying link compliance before tape-out demands efficient tooling. The module supports the standard, advanced, and 3D package types, adapting terminations, clock frequency, and voltage-transfer-function (VTF) methodology to the selected package and data rate. Statistical eye analysis with configurable rise time, swing, and sampling resolution yields insertion-loss and crosstalk pass/fail verdicts, mask-based eye

margin, and BER-versus-rate curves, providing an integrated compliance workflow for chiplet interconnect evaluation.

TITLE	**A Harmonic-Domain Electrical Modeling Framework for EMC and SI/PI Analysis**
TIME	14:30-14:45, November 5th
VENUE	QIER Hall, Haining Yuanzheng Hotel
AUTHORS	Alessandro Sona and Federico Tramarin (University of Padova, Italy)

ABSTRACT

Modern high-speed electronic systems are increasingly affected by SI/PI and EMC issues arising from the interaction between switching devices and the surrounding electrical network. Addressing these issues at the system level requires analysis tools that retain sufficient electrical detail while remaining compact and computationally efficient for practical investigations. In this context, this paper investigates a harmonic-domain electrical modeling framework based on an admittance representation of switching devices, interconnects, power distribution networks, return paths, and other passive and parasitic elements. The framework builds upon Augmented Equivalent Modeling (AEM) and exploits an Augmented Thevenin Model (ATM) to evaluate the effects of selected parameter variations on electrical quantities observed elsewhere in the network, without recalculating the complete network solution. A representative two-stage case study is considered to illustrate its engineering-oriented capabilities for SI/PI and EMC investigations.

OVERVIEW OF SESSION IV

SESSION	SS4 Intelligent Parametric Modeling and Inverse Design of Microwave Components and Metasurfaces
VENUE	HUANYING Hall (环瀛厅)
TIME	15:30-17:05 November 5th
SESSION CHAIRS	Jianan Zhang, Southeast University Feng Feng, Tianjin University Meng Meng Li, Nanjing University of Science and Technology
TECHNICAL TALKS	
15:30-15:50	**Physics-Guided Learning for Advanced 3D Packaging: From Thermal Simulation to Stress Prediction (Invited)** *Zhou Jin (Zhejiang University, China)*
15:50-16:05	**A Hybrid Physics-Machine Learning Framework for Data-Efficient and Scalable Parametric Modeling of Frequency-Selective Rasorbers (#1571358634)** *Meng Yuan Li and Jianan Zhang (Southeast University, China)*
16:05-16:20	**Data-Efficient Multiphysics Parametric Modeling of Frequency Selective Surfaces via Physics-Inspired Iterative Framework (#1571359190)** *Liaoyuan Xu and Jianan Zhang (Southeast University, China)*
16:20-16:35	**Conditional Diffusion-Based Inverse Design of Pixelated Metasurface Absorbers (#1571357809)** *Niting Mao and Jianan Zhang (Southeast University, China)*
16:35-16:50	**Gradient-Based Optimization for Rapid Beamforming of Coding Metasurfaces via Differentiable Quantization (#1571357550)** *Ziyi Zhang and Jianan Zhang (Southeast University, China)*
16:50-17:05	**Efficient Inverse Design of Metasurfaces for Multidimensional Electromagnetic Wave Control via Adjoint Sensitivity Based on the Discrete Dipole Approximation (#1571359212)** *Hao Li and Jianan Zhang (Southeast University, China)*

TITLE	**Physics-Guided Learning for Advanced 3D Packaging: From Thermal Simulation to Stress Prediction (Invited)**
TIME	15:30-15:50, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHOR	Zhou Jin (Zhejiang University, China)



ABSTRACT

As advanced 2.5D/3D packaging evolves toward higher power densities and increasingly complex multilayer heterogeneous integration, thermal effects and the resulting thermomechanical stresses have become critical challenges for performance and reliability. However, conventional high-fidelity numerical simulations are computationally expensive, limiting their applicability to rapid design exploration and optimization. This talk presents physics-guided AI modeling approaches for efficient thermal and stress analysis of advanced 3D packaging. First, a high-resolution thermal prediction framework for 3D ICs is introduced, combining coarse-mesh finite element analysis (FEA) priors with residual learning to enable fast and accurate temperature field reconstruction. Second, a full-chip thermal stress prediction method is presented, integrating multiphysics information from temperature distributions, material

properties, geometric structures, and interfacial characteristics to efficiently model complex stress fields in 3D packages. These studies demonstrate that combining physics-based simulations with AI-driven models can significantly improve the efficiency of thermal and reliability analysis, offering a promising pathway toward rapid design exploration and optimization of advanced semiconductor packaging.

BIOGRAPHY

Zhou Jin is a ZJU100 Professor at Zhejiang University. She obtained her Bachelor's degree from Nanjing University in 2010, followed by her Master's and Ph.D. degrees from Waseda University, Japan, in 2012 and 2015, respectively. Her research mainly focuses on VLSI circuit simulation and verification. She has published over 100 papers in top-tier international conferences and journals such as DAC, SC, PPoPP, ICCAD, TCAD, TODAES, TCAS-II, etc. She received the Best Paper Award at SC'23, Best Paper Nomination at SC'24/PPoPP'26/DATE'26, Honorable Paper Award at ISEDA'23, and Youth Science and Technology Award from EDA Ecosystem Development Accelerator in 2023, etc.

TITLE	**A Hybrid Physics-Machine Learning Framework for Data-Efficient and Scalable Parametric Modeling of Frequency-Selective Rasorbers**
TIME	15:50-16:05, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Meng Yuan Li and Jianan Zhang (Southeast University, China)

ABSTRACT

This paper presents a hybrid physics-machine learning framework for data-efficient parametric modeling and optimization of multi-layer frequency-selective rasorbers (FSRs). The framework integrates artificial neural networks (ANNs) with transmission line theory (TLT) to construct a neuro-TLT surrogate model. Full-wave simulations are first performed for individual lossy and lossless layers, from which their scattering matrices are extracted. Layer-level neural networks are then trained to learn the mappings between geometrical parameters and scattering matrices. By cascading the predicted layer responses through TLT, the model rapidly predicts the overall electromagnetic responses of multi-layer FSRs. The layer-wise architecture also allows trained models to be reused in new stacking configurations with shared layer topologies, reducing additional simulation and retraining costs. Two design examples demonstrate that the proposed method improves optimization efficiency over direct full-wave optimization and provides greater accuracy and structural reusability than purely data-driven ANN models. Numerical and experimental results validate its effectiveness.

TITLE	**Data-Efficient Multiphysics Parametric Modeling of Frequency Selective Surfaces via Physics-Inspired Iterative Framework**
TIME	16:05-16:20, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Liaoyuan Xu and Jianan Zhang (Southeast University, China)

ABSTRACT

Frequency selective surfaces (FSSs) are a class of periodic functional structures, which play an irreplaceable role in different areas. In practical engineering scenarios, FSSs are not in an ideal single-physics (EM-only) environment, but in situations involving complex coupling effects of multiple physical fields. However, the high resource intensity of multiphysics simulations makes accurate multiphysics FSS designs quite challenging. To address the aforementioned challenges, we propose a data-efficient multiphysics parametric modeling method of FSSs via physics-inspired iterative predictive framework. The proposed physics-inspired framework comprises two predictive networks, i.e., an EM network and a thermal network. Once the EM and thermal networks are pre-trained using single-physics data, the two networks iterate their predictions until temperature changes stabilize through the overall predictive framework. The proposed approach transfers the requirement for computationally expensive multiphysics data into a need for single-physics datasets, thereby considerably reducing the cost for developing an accurate multiphysics parametric model of FSSs. The effectiveness and advantages of the proposed method are demonstrated through numerical example using a bandpass FSSs.

TITLE	**Conditional Diffusion-Based Inverse Design of Pixelated Metasurface Absorbers**
TIME	16:20-16:35, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Niting Mao and Jianan Zhang (Southeast University, China)

ABSTRACT
The inverse design of pixelated absorbing metasurfaces is challenging because of the high-dimensional discrete design space, the intrinsic one-to-many mapping between electromagnetic (EM) responses and structures, and the high cost of repeated target-specific full-wave optimization. To address these challenges, this paper proposes a conditional-diffusion-based generation--screening--verification framework for high-degree-of-freedom (high-DOF) absorber inverse design. First, the desired absorber response is encoded by a compact masked target descriptor, which conditions a diffusion model to generate a distribution of feasible pixelated topologies. Second, a trained forward surrogate rapidly predicts the EM responses of the generated candidates and ranks them using a task-dependent screening score. Third, only the selected high-ranking candidates are evaluated by high-fidelity full-wave simulations for final verification. Different from inverse-design approaches that require a complete target response spectrum or repeatedly optimize a single structure for each specification, the proposed framework can flexibly accommodate different design requirements, preserve solution diversity and reduce reliance on repeated full-wave searches. The effectiveness of the proposed framework is demonstrated through both numerical studies and experimental characterization. Numerical studies involving one- to four-peak targets demonstrate accurate and diverse inverse designs, while comparisons with genetic algorithm (GA) and conditional variational autoencoder (CVAE) baselines show more consistent satisfaction of prescribed multi-peak constraints. Experimental characterization of a fabricated triple-peak absorber through free-space reflection measurements further confirms that the intended multi-resonant absorption behavior predicted numerically is retained in physical realization. These results demonstrate that the proposed framework provides an effective and extensible route for sparse-specification inverse design of high-DOF metasurface absorbers.

TITLE	**Gradient-Based Optimization for Rapid Beamforming of Coding Metasurfaces via Differentiable Quantization**
TIME	16:35-16:50, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Ziyi Zhang and Jianan Zhang (Southeast University, China)

ABSTRACT
Space-coding metasurfaces (SCMs) and space-time-coding metasurfaces (STCMs) manipulate electromagnetic waves through programmable meta-atoms with a finite set of discrete phase states, which renders the associated beamforming problem combinatorial and computationally prohibitive as the aperture size and time-coding length grow. Conventional heuristic solvers, such as genetic algorithm (GA) and simulated annealing (SA), suffer from low search efficiency in such high-dimensional discrete spaces, whereas analytical quantization of continuous weight distributions incurs considerable performance degradation under low-bit constraints. To address these challenges, we propose a differentiable quantization optimization (DQO) framework for rapid and high-quality beamforming of coding metasurfaces. By enabling gradient propagation through the discrete coding variables, the framework provides an explicit search direction at each iteration and thus achieves efficient exploration of the large-scale discrete design space. The effectiveness of the proposed method is demonstrated through several representative scenarios, including single-beam steering, flat-top synthesis, multi-beam generation, and multi-harmonic beam shaping, followed by experimental validation on a fabricated metasurface prototype covering both SCMs and STCMs. Compared with GA and SA, the proposed method consistently achieves lower peak sidelobe levels with an order-of-magnitude speedup, and remains tractable for design spaces with tens of thousands of discrete variables. Remarkably, for a 2-bit 20×32×32 STCM with an optimization space of 4^20,480 states, the proposed method completes the multi-harmonic beam-shaping task in only 1.76s. In contrast, GA and SA fail to achieve comparable performance even with substantially longer runtimes. These results establish differentiable quantization as a practical and scalable route toward real-time beamforming of large-scale coding metasurfaces.

TITLE	**Efficient Inverse Design of Metasurfaces for Multidimensional Electromagnetic Wave Control via Adjoint Sensitivity Based on the Discrete Dipole Approximation**
TIME	16:50-17:05, November 5th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Hao Li and Jianan Zhang (Southeast University, China)

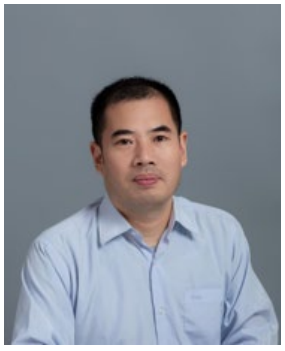
ABSTRACT

Metasurfaces enable a wealth of counterintuitive emergent electromagnetic (EM) phenomena through engineered arrangements of meta-atoms, and inverse design has become the leading approach for the autonomous exploration and optimization of such devices. However, prevailing inverse-design methods typically require extensive, time-consuming full-wave simulations at each iteration, or resort to theoretical equivalent models in place of full-wave simulations. Although such models accelerate computation, they often do so at the expense of circumventing or neglecting inter-meta-atom coupling and the dielectric interface effect, yielding candidate designs that are only near local optima or even entirely infeasible. Here, we recast the metasurface as a collection of "resonant particles" on a dielectric substrate, described by the full polarizability tensors and the planar-stratified dyadic Green's function. By solving the discrete dipole approximation equations, we faithfully capture inter-meta-atom coupling and the global EM response. On this basis, we further propose an adjoint-based optimization framework to achieve highly efficient topological inverse design of metasurface arrays. The proposed inverse-design paradigm greatly facilitates multidimensional, multi-degree-of-freedom electromagnetic wave control. We demonstrate its effectiveness and advantages by designing dual-polarization multi-frequency multiplexed and multi-frequency chirality-decoupled metasurfaces, all validated both numerically and experimentally. Our results show that the proposed framework delivers a modeling accuracy comparable to commercial EM solvers while achieving a speedup up to two orders of magnitude. This work establishes a new paradigm for the automated design of metasurface arrays and can be readily extended to the discovery and design of EM structures in other frequency regimes.

OVERVIEW OF SESSION V

SESSION	SS5 Advanced Printed Circuit Technologies at Millimeter-wave and Terahertz Technologies
VENUE	HUIYUAN Hall (慧源厅)
TIME	15:30-16:25 November 5th
SESSION CHAIRS	Yifei Zhang, Shandong University Weihong Liu, Xi'an University of Posts and Telecommunications
TECHNICAL TALKS	
15:30-15:50	**60-93.5 GHz Broadband Bond Wire Compensation Technique Based on DGS (#1571365689 Invited)** *Wei Hong Liu (Xi'an University of Posts & Telecommunications, China); Lei Zhou (XUPT, China)*
15:50-16:10	**Oxide Semiconductor Based Tunable Devices at Millimeter-Wave and Terahertz Frequencies (#1571353902 Invited)** *Yifei Zhang (Shandong University, China)*
16:10-16:25	**Heterogeneous Polymer Integration for High-Frequency Interconnects in Advanced Packaging Applications (#1571353745)** *Jian Song and Lei Chen (Shandong University, China); Tian Hao Ling (Aerospace Information Technology University, China); Yifei Zhang (Shandong University, China)*

TITLE	**60-93.5 GHz Broadband Bond Wire Compensation Technique Based on DGS (Invited)**
TIME	15:30-15:50, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Wei Hong Liu (Xi'an University of Posts & Telecommunications, China); Lei Zhou (XUPT, China)



ABSTRACT

To address the challenges of conventional wire bonding interconnects in millimeter-wave and terahertz system-in-package (SiP) heterogeneous integration, including high parasitic inductance, high-frequency impedance mismatch, limited operating bandwidth, and excessive signal loss, this paper proposes a novel ultra-wideband bond-wire impedance matching circuit based on a multilayer liquid crystal polymer (LCP) substrate. The proposed circuit innovatively integrates radial shorting stubs and microstrip lines to construct an impedance compensation structure. Furthermore, defected ground structure (DGS) units are symmetrically etched on the ground plane of the grounded coplanar waveguide (GCPW) to accurately compensate for the high-frequency parasitic effects introduced by bond wires. This approach effectively improves impedance matching performance and extends the signal transmission bandwidth. Experimental results demonstrate that the proposed circuit achieves excellent high-frequency transmission performance, with a reflection coefficient of $|S11| > 15$ dB and an insertion loss of $|S21| < 1.5$ dB over the frequency range of 60-93.5 GHz, corresponding to an ultra-wide operating bandwidth of 33.5 GHz. The proposed design effectively overcomes the limitations of conventional bond-wire interconnects, such as high transmission loss and narrow bandwidth at millimeter-wave frequencies, providing a promising solution for ultra-wideband and low-loss interconnects in millimeter-wave SiP heterogeneous packaging applications.

BIOGRAPHY

Liu Weihong: Associate Professor, Ph.D. in Electronic Science and Technology, and master's supervisor in Electronic Science and Technology and Electronic Information at Xi'an University of Posts and Telecommunications. He serves as a member of the Committee on Key Materials and Technologies for Electronic Components. His main research interests include the design of millimeter-wave active and passive

devices and RF integrated circuit design. From January to December 2019, he served as a visiting scholar at the National University of Singapore for 12 months.

TITLE	**Oxide Semiconductor Based Tunable Devices at Millimeter-Wave and Terahertz Frequencies (Invited)**
TIME	15:50-16:10, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Yifei Zhang (Shandong University, China)



ABSTRACT
As frequency increases up to millimeter-wave and terahertz regions, the conventional tunable devices meet many constraints, such as considerable dispersion, high insertion loss, low integration yield, etc. To address these issues, several oxide semiconductors with relatively low carrier mobilities have been monolithically fabricated on printed circuit boards, providing a new platform for tunable devices at millimeter-wave and terahertz frequencies.

BIOGRAPHY
Yifei Zhang received the B.S. and M.S. degrees in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2006 and 2009, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Delaware, DE, USA, in 2016. From 2016 to 2018, he was a post-doctoral research fellow at the School of Microelectronics, Shandong University, Shandong, China. He joined the School of Microelectronics, Shandong University, Shandong, China as an Associate Professor in 2018 and was promoted to Professor at the School of Integrated Circuits, Shandong University, Shandong, China in 2024.
He is currently the Qilu Professor, the Outstanding Scholar Professor, and the founder of the Tera-Millie Wave (TMW) group at Shandong University. His research interests include electrical circuits and electronic devices, dynamic metasurfaces, microwave-photonic devices, high-frequency integration and packaging, and their sensing and communication applications at terahertz and millimeter-wave frequencies. He has published more than 80 international articles and holds more than 10 international and Chinese patents

TITLE	**Heterogeneous Polymer Integration for High-Frequency Interconnects in Advanced Packaging Applications**
TIME	16:10-16:25, November 5th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Jian Song and Lei Chen (Shandong University, China); Tian Hao Ling (Aerospace Information Technology University, China); Yifei Zhang (Shandong University, China)

ABSTRACT
With the increasing demands of 5G millimeter-wave communications and high-speed data transmission, high-frequency interconnects in advanced packaging face challenges including high-frequency losses and parasitic effects. Heterogeneous integration of flexible polymer substrates with low-loss photosensitive dielectric layers offers both mechanical flexibility and fine patterning capability. In this work, benzocyclobutene (BCB) is used as the photosensitive dielectric and liquid crystal polymer (LCP) as the flexible substrate. BCB provides a low dielectric constant (~2.5-2.65), low loss tangent (0.0008), and excellent planarization, while LCP offers a low dielectric constant and low loss tangent with flexibility. BCB was spin-coated on plasma-pretreated LCP, and key parameters including spin speed, soft-bake temperature, and curing profile were optimized. Laser direct writing lithography defined patterns and vias, followed by oxygen plasma descum. The optimized process achieved a minimum line width of 3 μm, a minimum circular pattern diameter of 8 μm, and vias with a diameter of 18 μm and a sidewall angle of 68.5°. This heterogeneous polymer integration provides a viable path for high-density, high-frequency interconnects in advanced packaging, with potential for future terahertz applications.

OVERVIEW OF SESSION VI

SESSION	SS6 Signal Integrity and Equalization for AI and High-Speed Links
VENUE	HUANYING Hall (环瀛厅)
TIME	8:30-10:20 November 6th
SESSION CHAIRS	Shufang Li, Beijing University of Posts and Telecommunications Xiaohe Chen, China University of Petroleum (Beijing) Fayu Wan, Nanjing University of Information Science and Technology
TECHNICAL TALKS	
8:30-8:50	**Bandwidth vs. Loss Trade-off for PAM-n Modulations Toward 400 Gbps Data-Rates (#1571353293 Invited)** *Francesco de Paulis (University of L'Aquila, Italy); Sherman Shan Chen (Apple UK, USA); Tim Wang Lee and Mike Resso (Keysight Technologies, USA)*
8:50-9:05	**Intra-Pair Skew Modeling and Budgeting for Ethernet Based AI Rack Design (#1571347368)** *Yang Wu (Intel Corporation, China); Xinjun Zhang (Intel Asia-Pacific Research & Development Ltd., China); Weizhe Li (Intel Corp., China); Yinglei Ren (Intel Asia-Pacific Research & Development Ltd., China)*
9:05-9:20	**Impact of Fiber-Weave Effects on Differential Skew and PAM4 Eye Performance in High-Speed Interconnects (#1571353288)** *Yan Li (Cisco Systems, Inc., China); Felen Fu (Cisco Systems, Inc, China); Kai Li (Cisco Systems, Inc., China); Xiao-Ding Cai and Bidyut Sen (Cisco Systems, Inc, USA)*
9:20-9:35	**Link-Aware Distributed Negative-Group-Delay Phase Equalization for 112-Gb/s PAM4 Links (#1571353338)** *Xiang Fang and Fayu Wan (Nanjing University of Information Science and Technology, China); Blaise Ravelo (NUIST, China); Hongchuan Jia (Nanjing University of Information Science and Technology, China); Sébastien Lallechère (Université Bourgogne Europe & AFSCET, France)*
9:35-9:50	**Quad-Band Negative Group Delay Circuit for Inter Symbol Interference Suppression (#1571353575)** *Hongchuan Jia and Fayu Wan (Nanjing University of Information Science and Technology, China); Xiaohe Chen (China University of Petroleum, China); Blaise Ravelo (NUIST, China); Sébastien Lallechère (Université Bourgogne Europe & AFSCET, France)*
9:50-10:05	**Signal Integrity Analysis Framework and Design Optimization for PCIe 7.0 Interconnects (#1571358674)** *Harrison Xue (Lenovo, China); Boby Yan (Lenovo, USA); Zuli Qin and Zixiang Zhou (Cadence, USA); Yanwu Wang (DeTooLIC Ltd. Technology, China)*
10:05-10:20	**Signal Integrity Challenges of Rack-Scale CXL Memory Pooling Solution (#1571358828)** *Harrison Xue and Richard Li (Lenovo, China); Jiang Zhu and Jingwen Luo (Signal Easy, China); Yanwu Wang (DeTooLIC Ltd. Technology, China)*

TITLE	**Bandwidth vs. Loss Trade-off for PAM-n Modulations Toward 400 Gbps Data-Rates (Invited)**
TIME	8:30-8:50, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Francesco de Paulis (University of L'Aquila, Italy); Sherman Shan Chen (Apple UK, USA); Tim Wang Lee and Mike Resso (Keysight Technologies, USA)

ABSTRACT
The work presented in this paper aims at identifying an approximate trade-off between channel loss and required bandwidth for the high level amplitude modulation beyond PAM4, such as PAM6 and PAM8. The latter modulation formats may be potential candidates for the next generation of the Ethernet interfaces working above 400 Gbps. The analysis carried out in this paper takes into account the channel loss at Nyquist and the bandwidth reduction associated to PAM6 and PAM8 compared to PAM4 for deriving a theoretical limits in terms of channel length (loss) beyond which PAM4 is no longer convenient. These preliminary results set the base for a more comprehensive investigation involving a full-bandwidth analysis, thus including inter-symbol interference, and other impairments such as crosstalk, noise, jitter, with a properly optimized equalization architecture.

TITLE	**Intra-Pair Skew Modeling and Budgeting for Ethernet Based AI Rack Design**
TIME	8:50-9:05, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Yang Wu (Intel Corporation, China); Xinjun Zhang (Intel Asia-Pacific Research & Development Ltd., China); Weizhe Li (Intel Corp., China); Yinglei Ren (Intel Asia-Pacific Research & Development Ltd., China)

ABSTRACT
High-speed Ethernet links used in AI rack systems operate at 112 Gbps and above, making them highly sensitive to intra-pair skew. This paper analyzes the major skew sources in the full passive channel, including connectors, cables, PCB length-to-delay mismatch, and fiber-weave effects, and models their characteristics using ideal skew components by distributed cascading approaches. A full-channel COM-based assessment is developed to quantify skew tolerance independently of receiver variation. Based on skew sweeping across different channel segments, a practical skew budget is derived for an Ethernet AI-rack design, providing guidance for coordinating connector selection, cable specifications, and PCB routing to achieve cost-effective high-speed interconnect performance.

TITLE	**Impact of Fiber-Weave Effects on Differential Skew and PAM4 Eye Performance in High-Speed Interconnects**
TIME	9:05-9:20, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Yan Li (Cisco Systems, Inc., China); Felen Fu (Cisco Systems, Inc, China); Kai Li (Cisco Systems, Inc., China); Xiao-Ding Cai and Bidyut Sen (Cisco Systems, Inc, USA)

ABSTRACT
In this paper, a typical PCIe 6.0 PAM4 link is end-to-end simulated and the fiber-weave effect (FWE) on P/N skew and eye diagram is investigated. An equation-based algorithm is used to calculate S-parameters and Monte Carlo statistic method is performed to cover random weave offsets. Both skew and eye results show the advantage of taking large (≥10°) rotation and 2-ply structures, which provides industry with good references.

TITLE	**Link-Aware Distributed Negative-Group-Delay Phase Equalization for 112-Gb/s PAM4 Links**
TIME	9:20-9:35, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Xiang Fang and Fayu Wan (Nanjing University of Information Science and Technology, China); Blaise Ravelo (NUIST, China); Hongchuan Jia (Nanjing University of Information Science and Technology, China); Sébastien Lalléchère (Université Bourgogne Europe & AFSCET, France)

ABSTRACT
Residual nonlinear phase can persist after magnitude equalization in a 112-Gb/s PAM4 link and increase sampled intersymbol interference (ISI). This paper derives a complementary phase target from the complete magnitude-optimized baseline and realizes it with a differential distributed negative-group-delay (NGD) equalizer formed by two neighboring resistively loaded open stubs. The target is broad and shallow rather than tied to a prescribed 28 GHz resonance. A magnitude-matched control separates phase-specific benefit from attenuation and incidental magnitude shaping. For the nominal 15-dB at 28 GHz class (14.82 dB realized loss), the ADS model reduces sampled ISI by 70.54%, increases the signal-to-ISI ratio (SIR) by 5.31 dB, and enlarges the worst pre-DSP eye by 27.66%. At matched magnitude, 25.53% lower ISI and 1.28 dB higher SIR remain. The same equalizer is evaluated without retuning across a 10-20 dB MR-like channel family and with a fixed four-tap feed-forward equalizer (FFE) budget. A nominal four-port HFSS model confirms that the full-wave topology retains useful link-level improvement.

TITLE	**Quad-Band Negative Group Delay Circuit for Inter Symbol Interference Suppression**
TIME	9:35-9:50, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Hongchuan Jia and Fayu Wan (Nanjing University of Information Science and Technology, China); Xiaohe Chen (China University of Petroleum, China); Blaise Ravelo (NUIST, China); Sébastien Lalléchère (Université Bourgogne Europe & AFSCET, France)

ABSTRACT
This paper presents a quad-band negative group delay (NGD) circuit based on microstrip Spoof Surface Plasmon Polariton (SSPP) transmission lines. The quad-band resonance is achieved through the fano resonance between multi-stub resonators and the SSPP structure. The proposed circuit maintains excellent transmission performance at NGD frequencies while exhibiting good low-pass characteristics over a broad frequency range. With advantages of low loss and miniaturization, this circuit can be employed to compensate for group delay dispersion in transmission lines or channels, thereby reducing inter symbol interference.

TITLE	**Signal Integrity Analysis Framework and Design Optimization for PCIe 7.0 Interconnects**
TIME	9:50-10:05, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Harrison Xue (Lenovo, China); Boby Yan (Lenovo, USA); Zuli Qin and Zixiang Zhou (Cadence, USA); Yanwu Wang (DeTooLIC Ltd. Technology, China)

ABSTRACT
PCIe 7.0 increases PAM4 signaling to 128 GT/s, significantly tightening loss, crosstalk, discontinuity, and manufacturing constraints in server CPU-to-I/O interconnects. This work presents a unified design-for-manufacturing framework that translates electrical requirements into a compliance SerDes behavioral model and integrates package, PCB, via, connector, and cable optimization. Manufacturing robustness is incorporated through PCB material and trace loss optimization, via optimization and DOE/Monte Carlo analysis using UPM criterion. The deep via exhibits a statistically projected 0.84-dB insertion loss. End-to-end simulation of a challenging 500-mm cable/backplane topology, achieves feasible eye opening. The analysis establishes

preliminary interconnect solution spaces across PCB-, riser-, and cable-based server topologies. This enables quantitative PCIe 7.0 pathfinding while linking specification compliance, physical-channel optimization, manufacturing variation, high-volume system implementation.

TITLE	**Signal Integrity Challenges of Rack-Scale CXL Memory Pooling Solution**
TIME	10:05-10:20, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Harrison Xue and Richard Li (Lenovo, China); Jiang Zhu and Jingwen Luo (Signal Easy, China); Yanwu Wang (DeTooLIC Ltd. Technology, China)

ABSTRACT

Compute Express Link (CXL) enables coherent memory pooling and disaggregation, but rack-scale deployment requires interconnect reach beyond conventional PCIe topologies. This work presents an integrated PCIe 6.0-based methodology for a long reach CPU-to-switch CXL interconnect combining PCB and cable design, re-timer-based channel partitioning, active electrical cables (AECs), high-density OSFP-XD and thermal co-design. The original passive-copper topology die-to-die insertion loss, exceeding the PCIe 6.0 limit. Re-timer insertion splits the path into pre- and post-channel segments. Low-loss PCBs and optimized cabling preserve margin; OSFP-XD AEC cable and thermal optimization lowers simulated re-timer junction temperature. The combined SI-, cabling-, package-, and thermal-aware framework enables practical long-reach CXL memory pooling.

OVERVIEW OF SESSION VII

SESSION	SS7 Electromagnetic Measurement and Testing of Components and Systems
VENUE	HUIYUAN Hall (慧源厅)
TIME	8:30-10:10 November 6th
SESSION CHAIRS	Ge Shi, China Jiliang University Yan Li, China Jiliang University Zhipeng Xu, China Jiliang University Zhao Yuan, Chengdu University of Information Technology
TECHNICAL TALKS	
8:30-8:50	**Novel EMC Test Methods for Automotive-Grade Integrated Circuits (Invited)** **车规级集成电路电磁兼容测试新方法研究** *Jianfei Wu (Tianjin Institute of Advanced Technology, China)*
8:50-9:10	**Quantized Optical Lattice Constant-Based Nanometrology and Its Applications (Invited)** **量子化光晶格常数纳米计量技术与应用** *Xiao Deng (Tongji University, China)*
9:10-9:25	**A Novel ESD Test Platform for Electrode Moving Speed Effect Investigation (#1571346964)** *Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Yang Meng (China Academy of Science, China); Fang Wang, Xiaoye Fu and Wenli Wang (Guizhou Normal University, China); Yan li Chen (Tibet University, China)*
9:25-9:40	**TVS Harmonic Performance Evaluation with Communication Protocol Signals (#1571352631)** *Jingkun Mao (Tianjin University of Technology, China); John Xiao (Keysight, China & Keysight (China), China); Xiaohe Chen (China University of Petroleum, China)*
9:40-9:55	**Validation of the Temporal Correspondence Between Microcontroller Loop-Program Execution Timing and Electromagnetic Emissions (#1571353921)** *Kaipeng Yang, Junjie Wang, Yong Zhou and Yuan Zhao (Chengdu University of Information Technology, China)*
9:55-10:10	**A Circuit Defect Detection Method Based on Feature Space Local Anomaly Synthesis and Semi-Supervised Learning Mechanism (#1571347410)** *Zonghang Li, Yundi Liu and Tao Song (China Jiliang University, China); Linfeng Zhou and Mao Xiaoyuan (Shaoxing Test Institute of Quality and Technical Supervision, China); Songxiao Cao, Bin Zhou and ZhiPeng Xu (China Jiliang University, China)*

TITLE	**Novel EMC Test Methods for Automotive-Grade Integrated Circuits (Invited)** **车规级集成电路电磁兼容测试新方法研究**
TIME	8:30-8:50, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Jianfei Wu (Tianjin Institute of Advanced Technology, China)

ABSTRACT

As the level of electrification and intelligence in automobiles continues to advance, automotive-grade integrated circuits face an increasingly complex electromagnetic environment. Their electromagnetic compatibility (EMC) is directly related to vehicle driving safety and system reliability, which also poses higher demands on relevant testing technologies. This presentation focuses on EMC testing of automotive-grade integrated circuits. Through relevant case studies, it introduces the research progress and applications of testing technologies, discusses the current challenges and future development directions, and provides references for the research and practice of EMC testing of automotive-grade integrated circuits.

BIOGRAPHY

WU Jianfei, Ph.D. in Engineering, Professorate Senior Engineer, Deputy Chief Engineer of Tianjin Institute of Advanced Technology (TIAT). Currently serves as Deputy Director of the National IC-EMC Standards Working Group. Research areas: quantum microwave and electromagnetic compatibility (EMC) measurement of micro/nano devices, and EMC and reliability of integrated circuits. Over the past five years, he has led 12 projects including those under the 14th Five-Year Plan Common Technology Program; published 27 academic papers; obtained 14 authorized invention patents; authored 4 monographs; and led the development of 26 national EMC standards. Awards include: First Prize of Military Science and Technology Progress Award (ranked 5th), Grand Prize of Tianjin Science and Technology Progress Award (ranked 2nd), Third Prize of National Defense Science and Technology Progress Award (ranked 3rd), Tianjin Outstanding Young Talent, Outstanding Science and Technology Worker of the Chinese Institute of Electronics (CIE), and Tianjin May Fourth Youth Medal.

TITLE	**Quantized Optical Lattice Constant-Based Nanometrology and Its Applications (Invited)** **量子化光晶格常数纳米计量技术与应用**
TIME	8:50-9:10, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHOR	Xiao Deng (Tongji University, China)



ABSTRACT

Nanometrology is the foundation for precision measurement and quality control in integrated circuit manufacturing. Nanometrology technology based on quantized optical lattice constants uses the optical lattice constant as the main line for precise upward traceability and flattened downward dissemination, and has developed a series of key technologies, including directly traceable nanoscale length/angle reference materials, directly traceable grating interferometers and on-site calibration devices, and precision manufacturing technology for wafer-level reference wafers. This technology features directly traceable quantity values, high accuracy, strong robustness, and embedded calibration, providing a new approach for industrial on-site traceability.

纳米计量是集成电路制造精准测量与质量控制的基础。量子化光晶格常数的纳米计量技术以光晶格常数作为向上精准溯源和向下扁平化传递的主线，开发了一系列关键技术，包括：直接溯源型纳米长度/角度标准物质、直接溯源型光栅干涉仪及现场校准装置、以及晶圆级标准片精准制造技术等。该技术具备量值可直接溯源、精确度高、鲁棒性强、可嵌入式校准等特性，为产业现场溯源提供新思路。

BIOGRAPHY

Xiao Deng is a professor and doctoral supervisor at the School of Physics Science and Engineering, Tongji University, and deputy director of the National Integrated Circuit Micro-Nano Testing Equipment Industry Metrology and Testing Center (Shanghai). In 2024, Deng was selected as a National High-Level Young Talent. Deng has long been engaged in research on integrated circuit nanometrology and testing technology. As project leader, Deng has presided over projects under the National Key R&D Program and several General Programs of the National Natural Science Foundation of China. Distinctive research achievements include five national first-class certified reference materials (including China’s first nano-angle certified reference material). The research results have won the First Prize of the 2024 Shanghai Science and Technology Progress Award and the First Prize of the 2024 Science and Technology Progress Award of the Chinese Society for Measurement. In July 2026, as the second contributor, Deng won the First Prize of the 2025 National Science and Technology Progress Award.

邓晓，同济大学物理科学与工程学院教授，博士生导师，国家集成电路微纳检测设备产业计量测试中心（上海）副主任，2024 年入选国家高层次青年人才。长期从事集成电路纳米计量测试技术研究，作为项目负责人主持国家重点研发计划项目、基金委面上项目多项，特色研究成果为国家一级标准物质 5 项（含中国首个纳米角度标准物质）。研究成果荣获 2024 年度上海市科技进步奖一等奖、

2024 年度中国计量测试学会科学技术进步奖一等奖。2026 年 7 月，作为第二完成人荣获 2025 年度国家科学技术进步奖一等奖。

TITLE	**A Novel ESD Test Platform for Electrode Moving Speed Effect Investigation**
TIME	9:10-9:25, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Yang Meng (China Academy of Science, China); Fang Wang, Xiaoye Fu and Wenli Wang (Guizhou Normal University, China); Yan li Chen (Tibet University, China)

ABSTRACT
A new measurement system for noncontact electrostatic discharge (ESD) is designed and realized to study the electrode moving speed effect on discharge parameters. The system resolves the long-standing conflict: high-speed electrode approach for speed-effect research versus avoiding destructive collision. A theoretical model based on fluid conservation and Bernoulli's theorem is built for speed effect, and preliminary verification with gas-pressure and speed experiments is presented.

TITLE	**TVS Harmonic Performance Evaluation with Communication Protocol Signals**
TIME	9:25-9:40, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Jingkun Mao (Tianjin University of Technology, China); John Xiao (Keysight, China & Keysight (China), China); Xiaohe Chen (China University of Petroleum, China)

ABSTRACT
To evaluate transient voltage suppressor (TVS) harmonic behaviors under realistic operational conditions, comparing traditional continuous wave (CW) testing against complex protocol-level signals, the non-linear performance of two types of TVSs subjected to communication protocol signal excitation is investigated in this paper. The measurement process begins by evaluating the self-harmonics of the test setup to establish the noise floor of the system. Next, the non-linear harmonic performance of the two TVSs under CW stimulation is validated by benchmarking the results against officially published data. Finally, a real GSM communication protocol signal is applied as an excitation source to characterize non-linear performance under practical burst-signal conditions. The comparative results reveal that the non-linear harmonic distortion induced by periodic burst GSM signals is significantly more severe than that produced by standard CW excitation.

TITLE	**Validation of the Temporal Correspondence Between Microcontroller Loop-Program Execution Timing and Electromagnetic Emissions**
TIME	9:40-9:55, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Kaipeng Yang, Junjie Wang, Yong Zhou and Yuan Zhao (Chengdu University of Information Technology, China)

ABSTRACT
To validate the temporal correspondence between microcontroller program execution and near-field electromagnetic (EM) measurements, three loop test programs comprising different instruction types are used, and their theoretical loop periods are calculated from the instruction clock counts of the target device. After each program is downloaded to the microcontroller, the time-domain EM signal above the chip is acquired. The measured waveforms exhibit corresponding repetitive structures, and the variation in the repetition periods is consistent with the theoretical calculations. The results indicate that the acquired EM signals are temporally modulated by loop-program execution on the macroscopic time scale, providing a reliable timing reference for single-cycle segmentation, instruction-boundary calibration, and subsequent feature analysis.

TITLE	**A Circuit Defect Detection Method Based on Feature Space Local Anomaly Synthesis and Semi-Supervised Learning Mechanism**
TIME	9:55-10:10, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Zonghang Li, Yundi Liu and Tao Song (China Jiliang University, China); Linfeng Zhou and Mao Xiaoyuan (Shaoxing Test Institute of Quality and Technical Supervision, China); Songxiao Cao, Bin Zhou and ZhiPeng Xu (China Jiliang University, China)

ABSTRACT

To address overfitting from scarce circuit defect samples, complex background interference and difficult localization, this paper proposes a semi-supervised detection algorithm via feature-space local anomaly synthesis. It generates feature-level anomalies from defect-free samples to enhance generalization, embeds squeeze-and-excitation (SE) attention for small-defect perception, and adopts Wise Intersection over Union (WIoU) loss to optimize bounding-box regression. On the DeepPCB dataset, our model outperforms the baseline by 2.1\% in mAP@0.5 and 8.6\% in mAP@0.5:0.95 with AP gains across all six defect types, and surpasses mainstream detection approaches.

OVERVIEW OF SESSION VIII

SESSION	SS8 Advanced Computational Algorithms and Multiphysics Modeling for Integrated Systems
VENUE	YAXU Hall (雅叙厅)
TIME	8:30-9:35 November 6th
SESSION CHAIRS	Huan Huan Zhang, Xidian University Qiwei Zhan, Zhejiang University Haoqiang Feng, Zhejiang University
TECHNICAL TALKS	
8:30-8:50	**An Adaptive DG Method for Thermal Analysis of 3D Integrated Systems (#1571351838 Invited)** *Haoqiang Feng (Zhejiang University, China)*
8:50-9:05	**Multilevel Parallel DGTD Acceleration Using Asynchronous Remote Communication (#1571366496)** *Yunhao Qu (Nanjing University of Science and Technology,China); Qiran Lu (Nanjing University of Science and Technology, China); Hanyu Li and Haijing Zhou (Institute of Applied Physics and Computational Mathematics, China); Mengmeng Li (Nanjing University of Science and Technology & Communication Engineering, China); Dazhi Ding (Nanjing University of Science and Technology, China)*
9:05-9:20	**Electromagnetic Field Analysis of Chip Interconnects Using Enhanced High-Order DGTD Method (#1571354245)** *Zhenzuo Si, Haoqiang Feng and Qiwei Zhan (Zhejiang University, China)*
9:20-9:35	**AI-Driven Multiphysics Digital Twin and Closed-Loop Optimization for Thermal-Reliability-Aware Design of 3D Chiplet Systems (#1571353939)** *Honghao Jia and Qiwei Zhan (Zhejiang University, China)*

TITLE	**An Adaptive DG Method for Thermal Analysis of 3D Integrated Systems (Invited)**
TIME	8:30-8:50, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHOR	Haoqiang Feng (Zhejiang University, China)

ABSTRACT

Thermal analysis is important for the design of three-dimensional (3D) integrated systems, where complex structures and nonuniform heat distributions may require flexible numerical discretization. This paper presents an adaptive discontinuous Galerkin (DG) method for thermal analysis of 3D integrated systems. A local polynomial-order adaptation strategy is introduced to improve the numerical resolution in regions with relatively large errors. The polynomial order is adjusted according to a local error indicator, while lower-order approximation is retained in other regions. The proposed approach is applied to several thermal problems with nonuniform temperature distributions. Numerical results show that the adaptive DG method can provide accurate temperature solutions with reduced computational effort compared with uniform high-order discretization. The method provides a useful numerical approach for thermal modeling of 3D integrated systems.

TITLE	**Multilevel Parallel DGTD Acceleration Using Asynchronous Remote Communication**
TIME	8:50-9:05, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Yunhao Qu (Nanjing University of Science and Technology,China); Qiran Lu (Nanjing University of Science and Technology, China); Hanyu Li and Haijing Zhou (Institute of Applied Physics and Computational Mathematics, China); Mengmeng Li (Nanjing University of Science and Technology & Communication Engineering, China); Dazhi Ding (Nanjing University of Science and Technology, China)

ABSTRACT
This paper presents a multilevel parallel acceleration method for discontinuous Galerkin time-domain (DGTD) electromagnetic simulation on large unstructured meshes. The method combines Message Passing Interface(MPI) domain decomposition with asynchronous remote memory access (RMA) communication. MPI domain decomposition classifies element updates, according to data dependency, into interior element, local-face, and remote-face tasks. The CPU exchanges boundary ghost data through MPI RMA, while the heterogeneous computing unit executes batched local matrix-vector operations during the communication phase. Double buffering and degree-of-freedom reordering enable remote-face fluxes to be completed as neighboring data arrive. For a case with 26,214,272 tetrahedra, the method achieves up to 72% strong-scaling efficiency over 430,080 to 4,300,800 cores without altering the explicit DGTD formulation.

TITLE	**Electromagnetic Field Analysis of Chip Interconnects Using Enhanced High-Order DGTD Method**
TIME	9:05-9:20, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Zhenzuo Si, Haoqiang Feng and Qiwei Zhan (Zhejiang University, China)

ABSTRACT
Electromagnetic fields govern signal propagation, energy transport, and coupling in chip interconnects, making their spatial and temporal evolution essential to understanding signal integrity. As interconnect density and data rates increase, field interactions among conductors, dielectric layers, and return paths influence reflections, crosstalk, and signal distortion. Resolving these interactions provides the physical basis for interpreting terminal responses and identifying sources of signal degradation. This work applies a high-order discontinuous Galerkin time-domain (DGTD) method to investigate electromagnetic fields in multiscale chip interconnects, including through-silicon vias (TSVs) and serializer/deserializer (SerDes) channels. Maxwell's equations are discretized on unstructured tetrahedral meshes using local polynomial approximations and numerical fluxes, accommodating fine geometric details and heterogeneous material interfaces. Local time stepping assigns element updates according to local stability constraints, limiting the influence of refined regions on the temporal resolution elsewhere. Broadband excitation through lumped ports provides transient field distributions and terminal responses, from which scattering parameters are extracted. For TSVs, the analysis focuses on electric and magnetic field distributions around vertical transitions and coupling through the surrounding materials. For SerDes channels, it examines field interactions between neighboring signal paths and their relationship to transmission and crosstalk. Combining spatial field information with broadband port responses connects local electromagnetic behavior to interconnect performance. The study emphasizes the role of full-wave field analysis in understanding how interconnect geometry and material arrangement affect signal propagation. This DGTD approach provides a computational basis for examining electromagnetic interactions across chip interconnect structures and supporting signal integrity assessment in advanced integrated circuits and packaging.

TITLE	**AI-Driven Multiphysics Digital Twin and Closed-Loop Optimization for Thermal-Reliability-Aware Design of 3D Chiplet Systems**
TIME	9:20-9:35, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Honghao Jia and Qiwei Zhan (Zhejiang University, China)

ABSTRACT

The increasing integration density of 3D integrated circuits and chiplet-based systems creates severe thermal challenges, while repeated high-fidelity simulations remain computationally expensive for design-space exploration and reliability-oriented optimization. This work develops an AI-driven digital twin framework that integrates physics-based simulation, machine-learning surrogates, and adaptive multi-fidelity sampling for rapid thermal analysis and closed-loop optimization of 3D chiplet systems.

High-fidelity thermal simulations of representative multilayer chiplet architectures are used to train a surrogate model that reconstructs full-chip temperature fields rather than only scalar thermal metrics. This enables efficient evaluation of hotspot temperature, thermal gradients, hotspot location, and temperature nonuniformity. Adaptive sampling selectively enriches regions with high prediction error or uncertainty, reducing the need for expensive simulations. The current multiscale surrogate achieves a mean full-field temperature RMSE of approximately 1.99 K and a pooled R^2 of approximately 0.924, while maintaining reliable uncertainty-bound coverage across benchmark cases.

The trained digital twin is further embedded in an iterative design-simulation-verification-optimization loop for automated exploration of chiplet placement, power density, interface properties, and cooling parameters, providing a scalable basis for thermal-reliability-aware design and future multiphysics extension of advanced 3D integrated systems.

OVERVIEW OF SESSION IX

SESSION	SS9 AI-Assisted TCAD and EDA for Devices and Circuits
VENUE	YAXU Hall (雅叙厅)
TIME	9:40-10:25 November 6th
SESSION CHAIRS	Da-Wei Wang, Hangzhou Dianzi University Shuo Zhang, Zhejiang University Dan Shi, Beijing University of Posts and Telecommunications Yinliang Diao, South China Agricultural University
TECHNICAL TALKS	
9:40-9:55	**Physics-Constrained Neural Modeling of Dissipative Quantum Transport in Two-Dimensional MOSFETs and TFETs (#1571354348)** *Jintang Wang, Qi Shen, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)*
9:55-10:10	**Prediction of Far-Field Antenna Parameters Using Adaptively Sampled Spherical near-Field Data (#1571352039)** *Xiaodong Chen and Yinliang Diao (South China Agricultural University, China)*
10:10-10:25	**AI Modeling and Prediction of Electromagnetic Interference for Metamaterial-Shielded Precision Detection Environments (#1571353922)** *Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Ze Chen (Yancheng Teachers University, China); Kun Zhang (Institute of Mechanics, Chinese Academy of Sciences, China); Dandan Qu (Institute of Mechanics Chinese Academy of Sciences, China); Yang Meng (China Academy of Science, China)*

TITLE	**Physics-Constrained Neural Modeling of Dissipative Quantum Transport in Two-Dimensional MOSFETs and TFETs**
TIME	9:40-9:55, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Jintang Wang, Qi Shen, Wenzhang Fang and Shuo Zhang (Zhejiang University, China)

ABSTRACT

Two-dimensional transition-metal dichalcogenides (TMDs) offer atomically thin channels for heterogeneously integrated transistors, but at nanometer gate lengths confinement and scattering both dominate, so conventional drift-diffusion models become inadequate while ballistic models overestimate the on-current. The reference treatment - the non-equilibrium Green's function (NEGF) formalism coupled self-consistently to Poisson electrostatics and a scattering self-energy - is prohibitively expensive; Buttiker voltage probes make it tractable, ¨ with each probe chemical potential fixed by a zero-net-current condition. We report a three-band tight-binding model of a double-gate monolayer MoS2 n-type transistor, with the probe chemical potentials solved layer by layer: they barely perturb the electrostatic potential but nearly halve the channel carrier density, and the dissipative on-current is lower by a factor of about 2.7, with the subthreshold swing nearly unchanged. Finally, we formulate a physics-constrained neural surrogate as an outlook: it supplies initial states to the self-consistent loop, while the convergence criterion and the final solution remain with the solver. Index Terms-Physics-constrained machine learning, AIassisted TCAD, quantum transport, non-equilibrium Green's function, scattering, Buttiker probes.

TITLE	**Prediction of Far-Field Antenna Parameters Using Adaptively Sampled Spherical near-Field Data**
TIME	9:55-10:10, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Xiaodong Chen and Yinliang Diao (South China Agricultural University, China)

ABSTRACT
Spherical near-field (SNF) measurements are widely used for characterizing the far-field radiation properties of antennas. However, conventional spherical scanning typically requires a large number of uniformly distributed measurement points, resulting in considerable measurement time and effort. This study proposes an adaptive sampling approach for predicting far-field antenna parameters from sparsely sampled spherical near-field data. Measurement points over the spherical surface are adaptively selected using the method, allowing the sampling density to be adjusted according to the spatial characteristics of the measured near field. The acquired near-field data are then processed using a spherical near-field-to-far-field transformation to reconstruct the far-field radiation pattern of the device under test. The performance of the proposed approach is evaluated by comparing the reconstructed far-field results with those obtained using conventional uniformly sampled near-field data. The results demonstrate that the proposed adaptive sampling approach can reduce the number of required measurement points while maintaining good accuracy in the predicted far-field antenna characteristics, thereby improving the efficiency of spherical near-field antenna measurements.

TITLE	**AI Modeling and Prediction of Electromagnetic Interference for Metamaterial-Shielded Precision Detection Environments**
TIME	10:10-10:25, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Fangming Ruan (Guizhou Normal University, China & Www.gznu.edu.cn, China); Ze Chen (Yancheng Teachers University, China); Kun Zhang (Institute of Mechanics, Chinese Academy of Sciences, China); Dandan Qu (Institute of Mechanics Chinese Academy of Sciences, China); Yang Meng (China Academy of Science, China)

ABSTRACT
Accurate capture of weak magnetoencephalographic (MEG) signals for Alzheimer's-disease brain-science research places extreme demands on suppressing electromagnetic interference (EMI) across an exceptionally wide band, from hundreds of megahertz to sub-terahertz, while maintaining a stable zero-magnetic space. Traditional EMI analysis and shielding design rely on full-wave and multi-physics simulations that are computationally expensive, whereas measured shielding data remain sparse across metamaterial microstructures, incidence angles and frequency bands, which makes rapid EMI prediction and performance-driven design difficult. This paper proposes an AI-enabled EMI modeling and prediction framework tailored to metamaterial-shielded precision detection environments. First, a multi-source EMI dataset is constructed from measured shielding effectiveness (SE) of five non-metallic dielectric metasurface samples-including broadband SE from 0.95 to 18 GHz at different incidence angles, 2.6-40 GHz absorption and 75-210 GHz SE-together with 3-5 μm infrared absorption, impedance characterization and microwave imaging, and is augmented by multi-physics-coupled simulations of the metamaterial shielding chamber (1.23 m × 1.53 m × 1.89 m). A physics-informed deep surrogate model is then trained to map metamaterial microstructure parameters to broadband SE and the residual EMI distribution inside the chamber, replacing repeated full-wave solves and enabling inverse design of absorbing units. Preliminary results on held-out measurements show that the surrogate reproduces the measured SE characteristics-meeting the GJB 5792A-2021 Class C level from 100 MHz to 40 GHz, exceeding 75 dB at 75-110 GHz and 40 dB at 195-210 GHz-while reducing per-design prediction from hours of simulation to seconds and generalizing across incidence angles and microstructure variants. The framework provides rapid, data-driven EMI prediction and intelligent shielding design for weak-signal detection such as MEG and for typical electrostatic-protection scenarios in energetic-material forming processes, where electrostatic-discharge ignition hazards demand robust EMI/ESD suppression; it thereby opens an AI-metamaterial pathway for precision electromagnetic-compatibility and safety engineering.

OVERVIEW OF SESSION X

SESSION	SS10 Power Integrity and EMI Protection for Power Delivery Networks
VENUE	HUANYING Hall (环瀛厅)
TIME	10:40-11:55 November 6th
SESSION CHAIRS	Yusheng Hu, Jimei University Jiazheng Xu, ZTE Corporation
TECHNICAL TALKS	
10:40-10:55	**Power Tree Analysis with Multi-Phase Modeling and Nonlinear Converter Efficiency (#1571364152)** *Qiwen Yan (Southwest University of Science and Technology, China); Yin Sun, Yuteng Zheng, Mingjun Li and Xu Wang (DeTooLIC Technology Co., China); Xiaohe Chen (China University of Petroleum, China); Shufang Li (Beijing University of Posts and Telecommunications, China)*
10:55-11:10	**A Comparative Electrothermal Study of Vertical and Lateral Power Delivery in a Multilayer PCB (#1571364170)** *Hangkai Zhang (Zhejiang University, China); Xu Wang (DeTooLIC Technology Co., China); Xinglin Sun (Zhejiang University, China); Jun Fan (Missouri University of Science and Technology, USA)*
11:10-11:25	**Stopband Analysis of a Stepped-Impedance EMI Power Filter Using a Cascaded Network Model (#1571354367)** *Chenghao Lan, Yusheng Hu, Yudong Zhang and Yaoquan Ou (Jimei University, China)*
11:25-11:40	**Automated Modeling for On-Silicon PDNs: From GDS to Impedance (#1571370239)** *Jiahong Chen and Si-Ping Gao (Nanjing University of Aeronautics and Astronautics, China); En-Xiao Liu (Institute of High Performance Computing, Singapore); Wenjian Yu (Tsinghua University, China)*
11:40-11:55	**Graph Neural Network Surrogates for Coupled Electrothermal Analysis of 3D Power Delivery Networks (#1571353588)** *Jamila Rzali (Zhejiang University, China)*

TITLE	**Power Tree Analysis with Multi-Phase Modeling and Nonlinear Converter Efficiency**
TIME	10:40-10:55, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Qiwen Yan (Southwest University of Science and Technology, China); Yin Sun, Yuteng Zheng, Mingjun Li and Xu Wang (DeTooLIC Technology Co., China); Xiaohe Chen (China University of Petroleum, China); Shufang Li (Beijing University of Posts and Telecommunications, China)

ABSTRACT

This paper presents a steady-state power tree analysis method that jointly models the input-side and output-side branches of multi-phase DC-DC converters. User-defined nonlinear efficiency curves describe DC-DC conversion losses, while low-dropout regulators use a separate current-conserving model. Sink-current sweeps generate the overall power tree efficiency curve and quantify loss contributions from discrete components, voltage regulator modules, DC-DC converters, and low-dropout regulators. The method enables load-dependent assessment of power consumption and loss distribution across multistage power delivery networks.

TITLE	**A Comparative Electrothermal Study of Vertical and Lateral Power Delivery in a Multilayer PCB**
TIME	10:55-11:10, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Hangkai Zhang (Zhejiang University, China); Xu Wang (DeTooLIC Technology Co., China); Xinglin Sun (Zhejiang University, China); Jun Fan (Missouri University of Science and Technology, USA)

ABSTRACT
High-power processors in AI servers require large supply currents, and vertical power delivery (VPD) can shorten delivery paths to reduce voltage drop and distribution loss. This study compares VPD and lateral power delivery (LPD) models of the same PCB at 900A and an average CPU supply voltage of 0.800V. Compared with the LPD case, the VPD case has lower IR drop and 9.6W less power distribution network (PDN) loss, but a 15.1°C higher CPU peak temperature.

TITLE	**Stopband Analysis of a Stepped-Impedance EMI Power Filter Using a Cascaded Network Model**
TIME	11:10-11:25, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Chenghao Lan, Yusheng Hu, Yudong Zhang and Yaoquan Ou (Jimei University, China)

ABSTRACT
For high-frequency electromagnetic interference (EMI) isolation, this paper proposes a meandered electromagnetic bandgap (EBG) structure and analyzes its dispersion using a cascaded ABCD network model. Unlike stepped-impedance low-pass filters, the study focuses on the dispersion and multiple stopbands of a periodic structure. Equivalent shunt capacitances are introduced at the steps, and the dispersion relation is derived using Bloch-Floquet theory. COMSOL eigenfrequency results show that the model accurately predicts the lower-order stopbands below the higher-order-mode cutoff, providing a reference for EMI-oriented EBG design.

TITLE	**Automated Modeling for On-Silicon PDNs: From GDS to Impedance**
TIME	11:25-11:40, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHORS	Jiahong Chen and Si-Ping Gao (Nanjing University of Aeronautics and Astronautics, China); En-Xiao Liu (Institute of High Performance Computing, Singapore); Wenjian Yu (Tsinghua University, China)

ABSTRACT
This paper presents an automated modeling framework for aperiodic on-silicon power distribution networks (PDNs) directly from GDS files, enabling efficient impedance analysis and iterative PDN optimization. The proposed method first identifies repeated and connecting structures as unit cells from the GDS layout. Equivalent circuit models are employed for repeated unit cells, while full-wave electromagnetic analysis is employed for connecting unit cells. The resulting models are stored in a reusable database to avoid redundant extraction. The complete PDN model is then constructed by assembling the unit cells according to their connectivity in the GDS layout. The proposed method is validated using a multi-rail on-silicon PDN with lateral dimensions of 1.98×1.98 mm2. The proposed method achieves a 3.2× speedup without model reuse and reduces the computation time from 19,231 s to 0.516 s when previously extracted models are reused. Moreover, the proposed method captures mutual coupling between power rails, which is difficult to account for using the conventional equivalent circuit method alone. In all, the proposed framework facilitates efficient iterative optimization of on-silicon PDNs.

TITLE	**Graph Neural Network Surrogates for Coupled Electrothermal Analysis of 3D Power Delivery Networks**
TIME	11:40-11:55, November 6th
VENUE	HUANYING Hall (环瀛厅)
AUTHOR	Jamila Rzali (Zhejiang University, China)

ABSTRACT

This contribution presents a graph neural network surrogate for coupled electrothermal analysis of power delivery networks in 3D integrated systems. Coupled simulation of a copper interconnect stack, through-silicon vias, multi-level rails, micropliers and C4 bumps, resolves the temperature-dependent conductivity that links Joule heating to IR drop, but its cost makes it impractical inside design-space exploration, where hundreds of load and ground configurations must be evaluated. The proposed approach constructs a graph directly from the simulation mesh and predicts nodal potential and temperature rise jointly from geometry and boundary conditions alone, trained on coupled electric-current and heat-transfer solutions obtained with a commercial multiphysics solver. Generalization is assessed on unseen excitation maps, unseen die dimensions and unseen via-defect topologies, and the surrogate is compared against mesh-based and multiscale graph architectures.

OVERVIEW OF SESSION XI

SESSION	SS11 Physics-Based Modeling and Design Optimization of Interconnects and Wireless Systems
VENUE	HUIYUAN Hall (慧源厅)
TIME	10:50-11:50 November 6th
SESSION CHAIRS	Ping Li, University of Electronic Science and Technology of China Xiaochun Li, Shanghai Jiao Tong University Min Tang, Shanghai Jiao Tong University Yuxian Zhang, Anhui University Wei Wang, Hangzhou Dianzi University
TECHNICAL TALKS	
10:50-11:05	**RDL Interconnect Response Prediction via Parameterized Local-Model Reuse and Assembly (#1571363734)** *Yan Wang and Anqi Wang (Anhui University, China)*
11:05-11:20	**Physics-Based Inverse Methods for Impedance Corners and Material Extraction (#1571364597)** *Qihang Shang (DeTooLIC Ltd. Technology, China); Tianqi Zhou (Ningbo University, China); Wenzhi Wang (DeTooLIC Ltd. Technology, China)*
11:20-11:35	**Space Mapping Assisted Design Centering of High-Speed Connectors (#1571367205)** *Chaoqiang Zang (HUNAN University, China); Yuping Dan (xFusion Digital Technologies Ltd., China); Chi Lidong (Hunan University, China); Lei Deng (LinkE Technologies, China); Yinzhu Tang (Southwest University of Science and Technology, China); Yihong Qi (unknown)*
11:35-11:50	**A Dual-End Compact UWB Circularly Polarized Ring Patch Antennas (#1571353726)** *Wenzhe Gu, Xiong Yang and Yiyuan Luo (Huizhou University, China); Shiming Qin (Xi'an Aeronautical Computing Technology Research Institute, China)*

TITLE	**RDL Interconnect Response Prediction via Parameterized Local-Model Reuse and Assembly**
TIME	10:50-11:05, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Yan Wang and Anqi Wang (Anhui University, China)

ABSTRACT

Repeated electromagnetic simulations of redistribution-layer interconnects are costly even when the target structures share similar local features. This paper presents a parameterized local-response reuse and assembly method based on variable-length uniform transmission blocks and finite four-port junction blocks with variable corner radii. Geometric interface descriptions align cross sections, reference planes, and continuous return conductors, while assigning material loss to nonoverlapping local regions. At an independent junction observation point, the relative matrix error is 0.002285% at 1 GHz. For a four-port structure assembled from parameterized blocks, the complex relative errors of the reflection and through responses are 0.2219% and 0.07491% under the same native modal excitation and loading as the COMSOL reference. The resulting workflow combines response generation, physical interface connection, and network solution, providing numerical evidence for reusable local models and rapid prediction of similar interconnects.

TITLE	**Physics-Based Inverse Methods for Impedance Corners and Material Extraction**
TIME	11:05-11:20, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Qihang Shang (DeTooLIC Ltd. Technology, China); Tianqi Zhou (Ningbo University, China); Wenzhi Wang (DeTooLIC Ltd. Technology, China)

ABSTRACT
This paper presents two inverse workflows for PCB interconnect design. The first calculates impedance corners for DOE pre-simulation from a baseline design while respecting allowable parameter changes and optional limits on loss, delay, and crosstalk. Analytical first-order derivatives predict how changes in the active stackup, material, and conductor-geometry parameters affect impedance and enabled electrical limits. A constrained optimizer determines a candidate parameter set, and 2D FEM calculates the corresponding electrical response. A ten-conductor stripline case reached three impedance targets within 0.1 Ω in at most eleven iterations. The second converts S-parameters measured on uniform transmission lines into propagation constants γ, derives initial estimates of DK, DF, and roughness, and iteratively refines a selected material model with 2D-FEM evaluation. A closed-loop test achieved a maximum normalized γ residual below 5×10^{-4} in seven iterations.

TITLE	**Space Mapping Assisted Design Centering of High-Speed Connectors**
TIME	11:20-11:35, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Chaoqiang Zang (HUNAN University, China); Yuping Dan (xFusion Digital Technologies Ltd., China); Chi Lidong (Hunan University, China); Lei Deng (LinkE Technologies, China); Yinzhu Tang (Southwest University of Science and Technology, China); Yihong Qi (unknown)

ABSTRACT
A space mapping assisted design centering procedure is applied to a high-speed differential connector. A two-dimensional electrostatic coarse model is combined with residuals from converged HFSS simulations to estimate the probability that the differential characteristic impedance lies within 80 to 90 ohms under dimensional and material variation. Output calibration reduced held out impedance RMSE from 2.16 to 1.24 ohms across 81 inputs. Across 675 drawing grid centers, the mapped model predicts a 32 channel all pass probability of 86.30% for the selected candidate versus 73.23% for the nominal design under the independent channel assumption.

TITLE	**A Dual-End Compact UWB Circularly Polarized Ring Patch Antennas**
TIME	11:35-11:50, November 6th
VENUE	HUIYUAN Hall (慧源厅)
AUTHORS	Wenzhe Gu, Xiong Yang and Yiyuan Luo (Huizhou University, China); Shiming Qin (Xi'an Aeronautical Computing Technology Research Institute, China)

ABSTRACT
For outdoor follower vehicle positioning scenarios, this paper presents a UWB circularly polarized (CP) antenna designed for both handheld remote controllers and vehicular mobile terminals. The antenna features an annular radiating patch structure that integrates a central rectangular slot with 45-degree truncated corners. This design achieves miniaturization while covering an operating frequency band of 7.75-8.25 GHz. The measured results demonstrate $S_{11} < -10$ dB at both ports, port isolation $S_{21} < -25$ dB, peak gain ranging from 4.4 to 4.6 dBi, and 3-dB axial ratio (AR) bandwidth. Field tests indicate that the proposed antenna effectively mitigates polarization mismatch and environmental multipath interference. Consequently, it significantly enhances the link stability and ranging accuracy of mobile following systems. Furthermore, it has simple structure and low manufacturing cost.

OVERVIEW OF SESSION XII

SESSION	SS12 Advanced Multiphysics Analysis and Coupled-Physics Mechanisms
VENUE	YAXU Hall (雅叙厅)
TIME	10:50-11:50 November 6th
SESSION CHAIRS	Hua Guang Bao, Nanjing University of Science and Technology Yue Zhang, East China University of Science and Technology Tiancheng Zhang, Nanjing University of Science and Technology
TECHNICAL TALKS	
10:50-11:05	**A Finite-Difference-Based Fluid-Thermal Coupling Framework with SOR-Accelerated PISO for Microchannel Cooling in Power Amplifiers (#1571347088)** *Rengjun Zhou, Yan Peng, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)*
11:05-11:20	**An Accurate Electromagnetic-Fluid Multiphysics Model for High-Power Plasma Limiters (#1571348053)** *Dongming Liu, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China); Haoran Qin (Jiangsu University Of Science And Technology, China)*
11:20-11:35	**Three-Dimensional FDTD Method of Bidirectional Magneto-Mechanical Coupling in Magnetostrictive Layers of Magnetoelectric Antennas (#1571366499)** *Zheng Zhang, Lixia Yang and Yingsong Li (Anhui University, China); Chengjie Zuo (University of Science and Technology of China, China); Shitao Chen (Anhui University, China)*
11:35-11:50	**Intelligent Topology Optimization of Microstrip Ring Filters via Constrained Sampling Strategy (#1571347863)** *Chong Huang, Wen Fan, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)*

TITLE	**A Finite-Difference-Based Fluid-Thermal Coupling Framework with SOR-Accelerated PISO for Microchannel Cooling in Power Amplifiers**
TIME	10:50-11:05, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Rengjun Zhou, Yan Peng, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)

ABSTRACT

This work presents a bidirectional fluid-thermal coupling approach that combines a pressure-implicit with splitting of operators (PISO) solver with the finite-difference method to investigate microchannel cooling for power amplifiers mounted on a flat plate. The flow field is computed using a successive over-relaxation (SOR)-accelerated PISO algorithm for the pressure Poisson equation. After each thermal update, the dynamic viscosity is recalculated from the local temperature and returned to the momentum equations, thereby establishing bidirectional fluid-thermal coupling. Compared with COMSOL, the calculated velocity and temperature distributions show good agreement, with a maximum relative temperature error within 1%, while requiring only 48% of the computational time. These results demonstrate the accuracy and computational efficiency of the proposed approach.

TITLE	**An Accurate Electromagnetic-Fluid Multiphysics Model for High-Power Plasma Limiters**
TIME	11:05-11:20, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Dongming Liu, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China); Haoran Qin (Jiangsu University Of Science And Technology, China)

ABSTRACT
This paper presents an precise electromagnetic-fluid multiphysics model for high-power plasma limiters. Maxwell's equations and the electron-fluid equations are self-consistently coupled through the plasma current density. The local electric field governs electron momentum and energy, whereas the current determined by electron number density and mean drift velocity feeds back into the electromagnetic field. Furthermore, a spectral-element time-domain (SETD) discretization provides a high-order transient solution. The model is validated using the low-power S-parameters and high-power flat leakage power of a coaxial plasma limiter. The numerical and measured results are in agreement, demonstrating the correctness of the proposed method. The proposed method provides an effective numerical tool for the analysis and design of plasma limiters.

TITLE	**Three-Dimensional FDTD Method of Bidirectional Magneto-Mechanical Coupling in Magnetostrictive Layers of Magnetoelectric Antennas**
TIME	11:20-11:35, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Zheng Zhang, Lixia Yang and Yingsong Li (Anhui University, China); Chengjie Zuo (University of Science and Technology of China, China); Shitao Chen (Anhui University, China)

ABSTRACT
This paper proposes a three-dimensional finite-difference time-domain (FDTD) method for transient bidirectional magneto-mechanical coupling analysis in the magnetostrictive layer of magnetoelectric antennas. A coupled numerical framework is developed by integrating the elastodynamic and magnetic vector-potential equations through magnetostrictive constitutive relations. The physical quantities are arranged on a three-dimensional staggered grid, and local arithmetic averaging is employed to transfer coupling terms between different grid locations. The mechanical field is advanced using a second-order central-difference scheme, while the magnetic vector-potential equations are solved using sparse linear systems with the GMRES method. A three-dimensional cubic model subjected to a ramped harmonic body-force excitation is investigated. The calculated transient responses of Bz, Hz, uz, Tzz, and Szz show close agreement with those obtained using COMSOL Multiphysics, supporting the accuracy of the proposed coupling method. Furthermore, the proposed method achieves improved computational efficiency with reduced memory usage.

TITLE	**Intelligent Topology Optimization of Microstrip Ring Filters via Constrained Sampling Strategy**
TIME	11:35-11:50, November 6th
VENUE	YAXU Hall (雅叙厅)
AUTHORS	Chong Huang, Wen Fan, Tiancheng Zhang and Huaguang Bao (Nanjing University of Science and Technology, China)

ABSTRACT

This paper introduces a prior-knowledge-guided constrained Latin hypercube sampling (LHS) strategy and a corresponding topology optimization method, establishing a new paradigm for electromagnetic structure design. The proposed method extends the search space to a pixel-level discrete domain that accommodates topological variations. To manage this complexity, the approach first establishes a known baseline topology and then acquires dataset samples in a constrained manner. This strategy effectively broadens the design space while simultaneously compressing the search domain, which significantly reduces the dependence on a large training dataset. Compared with conventional electromagnetic simulation-based design methods, the proposed approach not only optimizes design objectives effectively but also accomplishes the microwave filter design in a significantly shorter timeframe. The efficacy of the method is validated through the design of a microstrip ring filter.

OVERVIEW OF YOUNG PROFESSIONALS FORUM

VENUE	**Venue: Qier Hall, Haining Yuanzheng Hotel** **Round-trip shuttle service will be provided. The shuttle will depart from the Hangzhou Blossom Water Museum Hotel at approximately 12:30 PM on November 5, after lunch, and return to Hangzhou after the session for the conference banquet that evening.** **地点：海宁圆正酒店启尔厅** **会议提供往返大巴接送。大巴将于 11 月 5 日午餐后约 12:30 从杭州宝盛水博园大酒店出发，活动结束后返回杭州，参加当晚的大会晚宴。**
TIME	15:30-17:00 November 5th
SESSION CHAIRS	Syed Muzahir Abbas, Macquarie University, Australia
INTRODUCTION	**Young Professionals Forum – Career Development and Growth Pathways** This session focuses on the professional development of young engineers, aiming to create an open and collaborative platform for sharing experiences and fostering mutual growth among early-career professionals. The discussion will revolve around three key topics: **1. Establishing a Clear Career Vision** – How can young professionals define their long-term career direction and develop a practical roadmap for continuous growth in the early stages of their career? **2. Developing Core Technical and Soft Skills** – What are the essential competencies that will shape the future of the electromagnetic and high-speed industries, and how can young engineers effectively enhance these skills to stay competitive? **3. Building and Sustaining Professional Networks** – How can young professionals actively cultivate high-quality connections and leverage professional communities to accelerate their career advancement? Through sharing experiences, challenges, and success stories, this session encourages participants to explore actionable strategies for achieving sustainable professional development in the dynamic field of electromagnetics.  



November 5, 2026 | **Qier Hall** Haining Yuanzheng Hotel | **Shuttle Service Provided** Departure: 12:30 PM

Technical Talks

13:30–13:45 **Double-Sides Launch Point Impedance Drift Correction for Accurate PCB Characteristic Impedance Measurement**
Wai Hong Chee, Brian Chi, Eason Yang

13:45–14:00 **Design and Tolerance Analysis of Differential Transmission Structures for High Speed Connectors**
Lei Deng, Lidong Cai, Licheng Li, Chaoqiang Zang, Yinzhu Tang, Lidong Chi, Yihong Qi

14:00–14:15 **Decomposition of Far-End Crosstalk in a Memory Channel**
Wenzhi Wang, Qihang Shang

14:15–14:30 **UCIe Link Compliance Analysis in a Multi-Functional S-Parameter Post-Processing Platform**
Zhifei Xu, Yajun Chen

14:30–14:45 **A Harmonic-Domain Electrical Modeling Framework for EMC and SI/PI Analysis**
Alessandro Sona, Federico Tramarin

Young Professionals Forum

15:30–17:00, November 5

· Join us for an open and collaborative discussion with young professionals from academia and industry.
· Share experiences, explore career pathways, and build your professional networks!

Key Topics

① **Establishing a Clear Career Vision**
② **Developing Core Technical and Soft Skills**
③ **Building and Sustaining Professional Networks**





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Shuttle Departure: 12:30 PM, Hangzhou Blossom Water Museum Hotel



OVERVIEW OF IBIS SUMMIT CHINA

VENUE	YUQING Hall (玉清厅)
TIME	8:30-12:25 November 6th
SESSION CHAIRS	Kinger Cai, Arm Limited, USA Ling Zhang, Zhejiang University, China
INTRODUCTION	The IBIS Summit is an international technical forum organized by the IBIS Open Forum, bringing together experts and engineers in high-speed system design, signal integrity, and modeling to discuss the latest standards and technology trends. IBIS Summit China is one of its key regional events, attracting leading companies and research institutes across China every year. In 2026, the IBIS Summit China will be concurrently held with the 2026 International Workshop on Advanced Interconnects (WAI 2026) in Hangzhou, China. This strategic partnership is aimed to synergize the two communities, with a focused exploration of cutting-edge topics on high-speed interconnects, SI/PI, and chip-package EMC. The joint event is expected to bridge the gap between standardization, academic research, and industrial application, accelerating innovations for the future of AI.
INVITED TALKS	**AI-Assisted Signal Integrity Analysis and Optimization for High-Speed Links** *Da-Wei Wang, Professor at Hangzhou Dianzi University, China* **Applying the IBIS-AMI Redriver Framework to Electrical-Optical-Electrical Links** *Andy Zambell at MathWorks, USA* **Efficient PDN Optimization Method Based on Equivalent Circuit Fine-Tuning** *Li Jiang, PhD Student at Zhejiang University, China* **ML for Practical PCB PDN Design** *Chulsoon Hwang, Associate Professor at Missouri University of Science and Technology, USA* **Theory and Techniques of RF Probe Calibration: From Parasitic Extraction of Calibration Standards to Calibration Algorithm** *Jiefeng Zhou at Nanjing University of Aeronautics and Astronautics, China* **A Phase-Noise-Based Method for Calculating Random Jitter Amplification in Clock Channels** *Tao Wei, PhD Student at Xidian University, China* **A Transformer-Driven Engine for High-Speed Interconnect Modeling and Multi-Objective Optimization in Seconds** *Yicheng Zhang, PhD Student at Zhejiang University, China*

TITLE	**AI-Assisted Signal Integrity Analysis and Optimization for High-Speed Links**
TIME	09:10 – 09:35, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Da-Wei Wang, Professor at Hangzhou Dianzi University, China

ABSTRACT

The growing complexity of high-speed interconnects in advanced packaging and 3D heterogeneous integration motivates AI-assisted approaches to improve the efficiency of signal integrity modeling, analysis, and optimization. This talk will present our recent research efforts in AI-assisted SI analysis and optimization for

high-speed interconnects, covering surrogate modeling, efficient simulation, and intelligent optimization techniques. Representative applications will be discussed to demonstrate how data-driven methods can be integrated with physics-based approaches to improve the accuracy and efficiency of SI analysis and design. Furthermore, considering the increasing interactions among electromagnetic, thermal, and power-related effects in advanced integrated systems, recent progress in multiphysics interconnect modeling, integrity analysis, and co-optimization will also be introduced. Finally, remaining challenges and future research directions toward AI-assisted design of high-performance integrated systems will be discussed.

TITLE	**Applying the IBIS-AMI Redriver Framework to Electrical-Optical-Electrical Links**
TIME	09:35 – 10:00, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Andy Zambell at MathWorks, USA

ABSTRACT
Linear-drive pluggable optics (LPO) and co-packaged optics (CPO) remove the retimer from the optical module, exposing the full electrical-optical-electrical (EOE) signal path to the host SerDes equalizer. Without the retimer to isolate domains, the Rx DSP must now equalize through optical impairments — ring modulator nonlinearity, photon-lifetime bandwidth limitations, and thermo-optic feedback — that behave fundamentally differently from the passive copper channels SerDes equalizers were designed for. Full system-level simulation becomes essential because these optical nonlinearities interact with the equalizer in ways that cannot be predicted by modeling the electrical and optical domains in isolation. A modern ADC-based SerDes with digital FFE/DFE responds to these impairments differently than a legacy analog CTLE/DFE architecture, and the only way to evaluate link margin for either is end-to-end co-simulation of the combined electrical-optical-electrical path. The IBIS-AMI standard already provides the framework to do this. This presentation demonstrates that the existing redriver topology is flexible enough to model an EOE link — including nonlinear, time-varying optical components — without any extensions to the standard. We discuss practical considerations for Init vs. GetWave partitioning when the channel includes inherently nonlinear elements, and how LTI approximations in Init can still produce useful equalization adaptation. Looking forward, we explore ideas for extending this approach: decomposing the optical domain into separate models — E-to-O conversion, fiber, and O-to-E conversion — to enable mix-and-match interoperability between vendors, and strategies for improving Init accuracy for nonlinear optical transfer functions.

TITLE	**Efficient PDN Optimization Method Based on Equivalent Circuit Fine-Tuning**
TIME	10:00 – 10:25, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Li Jiang, PhD Student at Zhejiang University, China

ABSTRACT
This work presents an efficient PDN optimization method based on equivalent circuit fine-tuning. A generalized inductance formulation is first derived for arbitrary pattern containing several power and ground vias. The exact current coefficients of different vias are then determined through rigorous theoretical derivation. An equivalent circuit model of PDN with a special property is then constructed or transformed from PDN S-parameters. When PDN structural modifications occur, the equivalent circuit is efficiently fine-tuned using the inductance variations obtained from the proposed inductance formulation. Case studies, including experimental measurements, corroborate the practicality and effectiveness of the proposed approach.

TITLE	**ML for Practical PCB PDN Design**
TIME	10:40 – 11:05, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Chulsoon Hwang, Associate Professor at Missouri University of Science and Technology, USA

ABSTRACT
With the growing complexity of modern hardware systems and increasingly short design cycles, there is a compelling need for faster, more efficient PDN design methodologies. Machine learning can play a pivotal role by enabling capabilities not possible with conventional approaches. This talk will introduce recent progress in machine-learning applications for PDN design, with a focus on practical PCB-level PDN design synthesis.

TITLE	**Theory and Techniques of RF Probe Calibration: From Parasitic Extraction of Calibration Standards to Calibration Algorithm**
TIME	11:05 – 11:30, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Jiefeng Zhou, Nanjing University of Aeronautics and Astronautics, China

ABSTRACT
Broadband on-wafer S-parameter measurement is essential for signal-integrity analysis of high-speed AI-chip channels, yet its accuracy is severely limited by RF probe parasitics, crosstalk, nonideal calibration standards, and complex error terms. This report presents a systematic calibration theory and technique for broadband on-wafer S-parameter measurement. It covers optimization-based parasitic extraction of calibration standards, a symmetric differential probe calibration method, and a 64-term error model for differential probe calibration up to 110 GHz. The proposed methods provide effective support for signal-integrity testing of high-speed AI-chip channels.

TITLE	**A Phase-Noise-Based Method for Calculating Random Jitter Amplification in Clock Channels**
TIME	11:30 – 11:55, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Tao Wei, PhD Student at Xidian University, China

ABSTRACT
As clock frequencies and data rates continue to increase, random jitter and its amplification through frequency-dependent interconnects have become important challenges in high-speed system design. This speech presents a phase-noise-based approach for analyzing and calculating random jitter amplification in clock channels. By incorporating the higher-order harmonics of realistic clock waveforms, the method provides a more accurate description of jitter propagation. The underlying mechanism of jitter amplification will be discussed in terms of the relative attenuation of jitter sidebands and clock harmonics. Simulation and measurement results from transmission lines and DDR5 channels will be presented to demonstrate the approach and illustrate how channel response, clock frequency, and jitter bandwidth influence jitter amplification. These findings offer practical insight for jitter budgeting, channel optimization, and timing-margin management in high-speed systems.

TITLE	**A Transformer-Driven Engine for High-Speed Interconnect Modeling and Multi-Objective Optimization in Seconds**
TIME	11:55 – 12:20, November 6th
VENUE	YUQING Hall @Level 1
SPEAKER	Yicheng Zhang, PhD Student at Zhejiang University, China

ABSTRACT

This talk presents a novel multi-objective inverse optimization method for high-speed interconnects based on a cascaded deep neural network (DNN) structure, enabling efficient simultaneous optimization of characteristic impedance, insertion loss, and far-end crosstalk (FEXT). Parameter optimization for high-speed interconnects is essential to ensuring signal integrity and electrical performance in complex designs such as multilayer printed circuit boards (PCBs) and chiplets. Conventional optimization approaches often require numerous iterations, making them highly time-consuming, especially in high-dimensional parameter spaces. In this talk, we introduce a DNN-based method that cascades an inverse-prediction network with a forward-prediction network to achieve multi-objective optimization by adjusting trace width, trace spacing, and pair-to-pair distance. Furthermore, we demonstrate how integrating integer programming enables the optimization of multilayer PCB stack-ups and the design parameters of individual signal layers within seconds, significantly improving efficiency compared with conventional optimization approaches.

POSTER SESSIONS

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
1	1571347054	A Preconditioned Domain Decomposition Framework for Multiphysics Analysis of RF Devices	*Huan Wang, Wenwei Zhang, Wenchi Huang, Jianing Cao, Jiaqi Kang, Chenche Zhao, Mingyao Xia*	*Peking University, China*
2	1571351036	Efficient Broadband Modeling of High-Speed Fixtures Using an Enhanced Stub Model	*Tao Zhou, Xu Wang, Bo Pu, Yanwu Wang, Jun Fan*	*Southwest University of Science and Technology, China; DeTooLIC Ltd. Technology, China; Missouri University of Science and Technology, USA*
3	1571352562	Double-Layer Triple-Band Circularly Polarized Reflectarray Antenna Producing Five Beams	*Lingfeng Xu*	*Nanjing University of Science and Technology, China*
4	1571354009	Machine-Learning-Assisted Wafer-Scale Prediction of IGZO Thin-Film Thickness Distributions Using a DeepONet Surrogate Model	*Junwei Wang, Chenyang Sun, Zhiyu Ma, Yi Li, Jie Liang*	*Shanghai University, China*
5	1571354070	Hybrid Bayesian Work Function Design for Symmetric RFETs	*Chenyang Sun, Junwei Wang, Zhiyu Ma, Jie Liang, Yi Li*	*Shanghai University, China*
6	1571354103	Reducing Low-Frequency CM Noise in Power Converters by Digital Active Closed-Loop Control	*Wenqi Lin, Qidong Bao, Xinglin Sun*	*Zhejiang University, China*
7	1571354231	Process-Sequential Modeling of TCB and Underfill Curing for 2.5-D Micro-Bump Interconnects with AI-Assisted Parameter Exploration	*Jiachen Yang*	*Hangzhou Dianzi University, China*
8	1571355571	Using a Spatial Null to Test Scalar Electric-Field Probe Interpretation	*Zipeng Chen, Wenxiao Fang, Huachun Wang*	*Sun Yat-sen University, China*
9	1571358782	Reusable GNNs for S-Parameter Extraction and SI Optimization of Coupled PCB Interconnects	*Junjie Peng, Ping Li*	*University of Electronic Science and Technology of China, China*
10	1571359628	Feasibility-First Two-Stage Optimization for Target-Impedance-Constrained PDN Decap Design	*Qiyu Jiang, Shufang Li, Xiaohe Chen*	*Beijing University of Posts and Telecommunications, China; China University of Petroleum (Beijing), China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
11	1571359650	Noise Coupling in Multilayer PCBs: Mechanism Analysis and Simulation-Measurement Correlation	*Cailiang Fu, Anfeng Huang, Yin Sun*	*Southwest University of Science and Technology, China; DeTooLIC Technology Co., China*
12	1571359868	Mapping Multiple Noise-Source Contributions from Synchronous near-Field Scans	*Hailing Zhao*	*Southwest University of Science and Technology, China & Mianyang, China*
13	1571360218	Impact of Frequency-Dependent High-Voltage Port Impedances on Vehicle-Level Radiated-Emission Prediction for Electric Vehicles	*Leixin Li, Li Zhai, Haonan Xu*	*Beijing Institute of Technology, China*
14	1571360270	Experimental Study of the Effect of High- and Low-Voltage Crosstalk on Common-Mode Interference Current in an Automotive FlexRay Bus	*Haonan Xu, Li Zhai, Leixin Li*	*Beijing Institute of Technology, China*
15	1571363991	Residual Neural Network for Tabbed-Routing Impedance Prediction in via Pin Fields	*Ren Qingyuan, Jie Li, Qihang Shang*	*City University of Hong Kong, Hong Kong; Southwest University of Science and Technology, China; DeTooLIC Ltd. Technology, China*
16	1571364740	Impedance Correction for PCB de-Embedding at 50 GHz and Above	*Anfeng Huang, Cailiang Fu*	*DeTooLIC Technology Co., China; Southwest University of Science and Technology, China*
17	1571365103	PDN Power-Plane Shape Optimization Through Vertex-Based Expansion for DC Impedance Reduction	*Chenxu Zhang, Ling Zhang, Er-Ping Li*	*Zhejiang University, China*
18	1571366768	Thickness-Constrained Design of Silicone-Bonded Nanocrystalline Sheets with Prescribed Magnetic Response	*Qiusen He, Bing Sun, Xiaoping Li, Xinglin Sun*	*Zhejiang University, China; Tianjin University, China; Swust University, China*
19	1571367232	FDTD Solution of the Landau-Lifshitz-Gilbert Equation for Ferromagnetic Resonance Simulation	*Zhidan Qiu, Shitao Chen, Lixia Yang, Yingsong Li, Chengjie Zuo*	*Anhui University, China; University of Science and Technology of China, China*
20	1571367415	Extraction of Parameters for the GaN Physics-Based Compact Model Based on Multi-Constraint Fitting	*Junhao Shen*	*Nanjing University of Science and Technology, China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
21	1571367694	Wideband Duplexer for EMC-Related Test Applications	*Wen Tao, Xiong Chen*	*Xi'an Jiaotong University, China; Xian Jiaotong University, China*
22	1571368429	Band-Specific Matching Networks for Broadband High-Power Amplifiers	*Zhengmin Chen, Xiong Chen*	*Xi'an Jiaotong University, China; Xian Jiaotong University, China*
23	1571369558	Thermal Dissipation of GaN Power Chip Package With Heat Slug on Die	*Shuaifei Wang, Jicun Lu, Miaosen Yang, Ruishuang Yuan*	*Shanghai DianJi University, China*
24	1571369748	Pulsed Magnetic Field Immunity of Six-Axis Force Sensors	*Xin Cheng, Ying-Hua Zhang, Xinxin Tian, Weiheng Shao, Mingbin Hu, Shao E*	*Guangdong University of Technology, China; Maritime Safety Administration, China; CEPREI Laboratory, China; China Electronic Product Reliability and Environmental Testing Research Institut, China; China Electronic Product Reliability and Environmental Testing Reasearch Institute, China*
25	1571369856	Solder Joint Quality and Reliability of Perforated Cu Clip in Power Module Package	*Penglin Zhang, Jicun Lu, Miaosen Yang, Ruishuang Yuan*	*Shanghai DianJi University, China*
26	1571369902	Event-Resolved Conducted EMI of Top-Side Interconnects in a Si/SiC Hybrid Switch	*Xinzheng Hu, Shaotong Yang, Yan Li*	*China Jiliang University, China*
27	1571369962	Equal-Area Pattern Redistribution in a Three-Layer Broadband Microwave Absorber	*Hualei Zhu, Longping Chen, Yan Li*	*China Jiliang University, China*
28	1571370822	Efficient Markov Simulation of Error Bursts in Coded Wireline Links	*Yuhao Huang, Hanrui Huyan, Xiuqin Chu*	*Xidian University, China; Xi'an University of Electronic Science and Technology, China*
29	1571370915	Hierarchical Volterra Modeling for Nonlinear High-Speed I/O Circuits Using DC/AC Characterization	*Yajun Lv*	*Xidian University, China*

NO.	PAPER ID	TITLE	AUTHORS	AFFILIATION
30	1571370947	Thermal Optimization of Si MOSFET Power Package on Solid-State Circuit Breaker PCB Board	*Tao Zhou, Bowen Yang*	*Shanghai DianJi University, China*
31	1571370953	CER-Aware FEC Redundancy Optimization for PAM4 Chiplet Links With DFE-Induced Error Propagation	*Yuhao Huang, Shen Chun, Xiuqin Chu*	*Xidian University, China; Xi'an University of Electronic Science and Technology, China*
32	1571371028	UV-Assisted Thermal Debonding of a Dynamic Alkoxyamine Wafer Temporary Adhesive	*Rui Li, Jicun Lu*	*Shanghai DianJi University, China*
33	1571371069	Effects of Conventional Annealing on the Magnetic Properties and Giant Magnetoimpedance of Co-Based Magnetic Microwires	*Shihong Mo, Jicun Lu*	*Shanghai DianJi University, China*
34	1571371078	Design and Characterization of Coplanar Nested-Coil FPC Transformers	*Tian Yang, Weisi He*	*Shanghai DianJi University, China*
35	1571371083	Statistics Supply Voltage Noise Calculation for Chip Under Logic Constraints	*Haiyue Yuan, Yuhao Huang, Yajun Lv, Yuhuan Luo, Jun Wang, Feng Wu, and Xiuqin Chu*	*Xidian University, China*
36	1571347798	Electromagnetic Interference Characterization of Integrated Circuits Based on near-Field Scanning and Dipole Reconstruction Techniques	*Han Dong-Hao; Xing-Chang Wei*	*Zhejiang University, China*

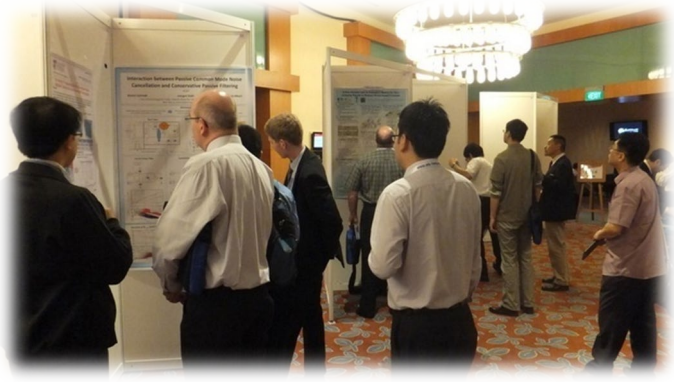
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Please register at the Registration Desk before proceeding to locate your assigned poster board. To locate your assigned poster board, look for the board marked with your Paper ID.

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- ☐ Each presenter is provided with a 2.4 meter-high by 1 meter wide poster board.
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- ☐ Poster setup should be completed before 3:30 p.m. on November 5th.
- ☐ Please make sure that your paper number is clearly visible on your poster board.
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Recommendations for other hotels:

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Hotel Name：

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Hotel Name：

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ABOUT HANGZHOU

Historical Significance




Hangzhou is a big city steeped in a rich, millennium-long history and is celebrated as one of China's seven ancient capitals. Central to its cultural legacy is the West Lake, a UNESCO World Heritage Site that has inspired poets, scholars, and artists for centuries and stands as a timeless symbol of Chinese aesthetic harmony. The city's heritage is further underscored by the Grand Canal, the world's longest man-made waterway, highlighting Hangzhou's enduring role as a vital nexus of historical commerce and vibrant cultural exchange.

Strategic Location




Situated on the southeastern coast of China, Hangzhou serves as the political, economic, and cultural center of Zhejiang Province. Nestled at the southern core of the Yangtze River Delta—one of the world's most economically dynamic regions—the city boasts a highly advantageous geographic position. It is seamlessly connected to Shanghai to the northeast and Ningbo to the east, making it a pivotal transportation and logistics hub that effectively bridges domestic networks with global markets.

Economic Development & Innovation





Hangzhou is globally recognized as a premier hub for the digital economy, technological innovation, and modern entrepreneurship. Often referred to as China's "Silicon Valley," it is home to world-renowned technology enterprises such as Alibaba and a thriving ecosystem of high-tech startups and research institutions. Supported by a robust advanced manufacturing sector, comprehensive e-commerce infrastructure, and a strong commitment to green and sustainable development, Hangzhou continues to be a leading driver of China's modern economic growth and innovation.

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